



Critical Techniques for High Speed A/D Converters in Real-Time Systems

Sixth Edition

A/D Markets and Technology
Sampling and Filtering Techniques
FPGA Technology
Switched Serial Fabrics
Products
Applications
Links

by

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Preface

An A/D (analog-to-digital) converter, frequently abbreviated as ADC, accepts an analog voltage at the input and produces a digital representation of that voltage at the output that's called a "sample".

The two primary characteristics of A/Ds are the rate of conversion or sampling rate, expressed in samples per second, and the accuracy of each digital sample expressed as the number of binary bits or decimal digits per sample.

Sampling rates vary tremendously between applications. A digital medical thermometer may deliver samples to update the readout once every five seconds while a high-speed wideband radar may produce 2 billion samples per second.

The difference in sample rates between these two prominent examples is a staggering 10 orders of magnitude. There are thousands of A/D applications spread continuously throughout this range.

To help define the meaning of "high-speed A/D" used in this handbook, we will be focusing primarily on A/D converters with sampling rates higher than 100 MHz. We will review sampling techniques, FPGA technology and high-speed serial fabrics. Finally, we will present the latest Pentek high-speed A/D products and applications based on them.

A/D Markets and Technology

High Speed A/D Converter Markets

- | | |
|---------------------------|----------------------------|
| ▪ Commercial Wireless | ▪ Wireless Networks |
| ▪ Military Communications | ▪ Control Systems |
| ▪ Radar | ▪ Signals Intelligence |
| ▪ Sonar | ▪ Medical Imaging |
| ▪ Telemetry | ▪ Military Countermeasures |
| ▪ Beamforming | ▪ Nuclear Instrumentation |
| ▪ Direction Finding | ▪ Structural Analysis |

Figure 1

Markets for high-speed A/D converters are significant in size and many are growing rapidly. New markets emerge regularly based on A/D technology advances, lower costs, and the general trend of replacing older mechanical and analog systems with DSP (digital signal processing) systems.

DSP offers significant advantages for handling signal complexity, communications security, improved accuracy and reliability, reduced size, weight and power.

Commercial users of high-speed A/Ds include wireless mobile communication systems, airline radar systems, air traffic control towers, ship communications, and wireless networks for home, office and public facilities.

Industrial uses include medical imaging systems and process control systems for manufacturing.

Government systems account for many of the high-end applications such as phased-array military radar, communications countermeasure systems, global military radio networks, unmanned aerial vehicles and intelligence gathering systems.

New Monolithic A/D Technology

- Smaller geometry, lower core voltages and power dissipation
- Much higher sample rates and bit accuracy
- Wideband input circuitry optimized for direct IF sampling
 - IF (intermediate frequency) signals are usually greater than F_s
 - Differential, transformer coupled inputs minimize noise
- High Performance Integrated S&H (sample-and-hold)
 - Higher immunity to clock waveform symmetry and level
- Improved multi-stage flash conversion techniques
- Digital sample code generation and error correction
 - Devices can be calibrated and trimmed during production
- Improved thermal tracking of DC offset, gain, and linearity
- Improved power supply noise rejection and immunity

Figure 2

Because of the complexity of these market segments, wideband A/D converters have made significant advances in recent years.

This is due partly to silicon process improvements and also to many applications that require direct sampling of IF signals well above 100 MHz.

One of the most important advances is the sample-and-hold (or track-and-hold) circuitry at the front end.

Just as important, are new sample clock interfaces and drivers.

At these speeds, you need state-of-the-art flash and multistage flash conversion techniques.

New techniques in digital error code correction and thermal compensation circuitry help eliminate errors in bit accuracy, linearity and gain.

Lastly, these new devices are more immune to power supply and system noise.

A/D Markets and Technology

Monolithic A/Ds for $F_s > 100$ MHz, bits ≥ 8

Monolithic A/D Converters					
Manufacturer	Part No.	Sample Freq.	Channels	Bits	Input BW
Atmel	AT84AS008	2,000 MHz	1	10	3,000 MHz
Maxim	MAX108	1,500 MHz	1	8	2,200 MHz
National	ADC08D1000	1,000 MHz	2	8	1,700 MHz
Atmel	AT84AD001B	1,000 MHz	2	8	1,500 MHz
Maxim	MAX101A	500 MHz	1	8	1,200 MHz
Atmel	AT84AD004	500 MHz	2	8	1,000 MHz
Texas Instr.	ADS5463	500 MHz	1	12	750 MHz
Texas Instr.	ADS5474	400 MHz	1	14	750 MHz
Texas Instr.	ADS5485	200 MHz	1	16	300 MHz
Analog Dev.	AD9480	250 MHz	1	8	400 MHz
Analog Dev.	AD9430	215 MHz	1	12	700 MHz
Analog Dev.	AD9410	210 MHz	1	10	500 MHz
Analog Dev.	AD9054	200 MHz	1	8	350 MHz
Linear Tech.	LTC2255	125 MHz	1	14	300 MHz

Figure 3

Shown in the table above are some representative examples of commercially available, monolithic A/D converters with sampling rates greater than 100 MHz and resolution of at least 8 bits.

All these devices are potential candidates for board-level products for embedded systems, such as those made by Pentek.

We have listed the input bandwidth in this table to highlight the importance of these A/Ds in direct IF sampling applications, also known as undersampling.

In the next section, we'll discuss in some detail the principles and rules of sampling.

Sampling and Filtering Techniques

Direct Baseband RF Signal Acquisition

- Antenna signals are usually in the microvolt range
- RF amplifier boosts signal to full scale input voltage of the A/D - usually 0 to +10 dBm
- RF amplifier often includes a tuned bandpass filter centered on the signal of interest
- No analog frequency translation before the A/D
- Appropriate for HF signal frequencies (3 - 30 MHz)

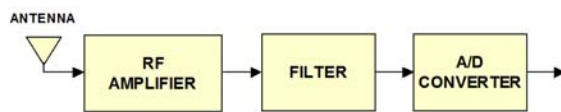


Figure 4

Most receiver systems start with a signal originating from an antenna that's often in the microvolt level, so it must first be amplified by an RF amplifier stage.

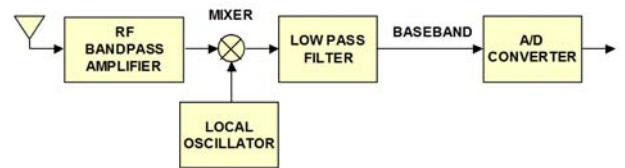
The amplifier is usually a tuned RF circuit which only passes the frequency band of interest, providing signal gain within that band and rejecting noise and unwanted signals in adjacent frequency bands.

If the RF input signal is at a low enough frequency, it can be digitized directly by an A/D converter, and no analog translation is necessary.

For example, you can usually perform direct baseband sampling on HF signals with no translation required, since the frequency content is below 30 MHz.

Analog RF Frequency Translation

▪ Analog Translation to Baseband



▪ Analog Translation to IF (Intermediate Frequency)

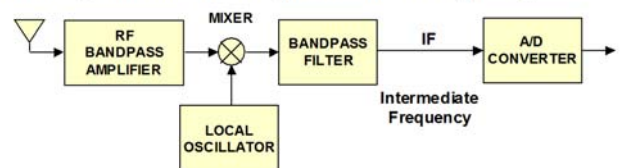


Figure 5

In the case where the antenna signal frequency is too high to be digitized directly by the A/D converter, it has to be translated down using an analog mixer and local oscillator.

The top diagram shows a simplified representation of this analog translation to baseband with a low pass filter following the mixer.

The bottom diagram shows the translation to an intermediate frequency or IF — this is quite common. In this case, the filter is a bandpass filter centered at the IF frequency.

So far, we've discussed three types of front end circuitry:

- 1) Direct sampling with no translation
- 2) Analog translation to baseband
- 3) Analog translation to IF

But how do we design the filters in each case?

Let's go back to review some fundamental sampling theory.

Sampling and Filtering Techniques

Filtering Helps Avoid Noise and Aliasing

- In all systems, the A/D input must be filtered for two important reasons:
 - Eliminate out of band noise
 - Eliminate aliasing
- Nyquist sampling theorem requires the input signal bandwidth must be less than one-half the sampling rate of the A/D converter
- Some systems (like an IF stage) provide inherent bandlimiting before the A/D
- Fundamental Sampling Modes
 - Baseband Wideband Sampling
 - Baseband Pre-select Sampling
 - Undersampling

Figure 6

Filters ahead of the A/D are needed primarily for two reasons: to eliminate out-of-band noise and to eliminate out-of-band signals that can cause aliasing.

Nyquist tells us that whenever you sample a signal with an A/D, the bandwidth of that signal must be less than half the sampling frequency of the A/D.

Filters help us guarantee that this rule is met. Sometimes the bandwidth is already limited by the signal source, like the output of an IF stage that takes advantage of the IF filter bandwidth. But each case has to be analyzed individually.

The design of the filter is also critically linked to the sampling mode. Here we've listed three fundamental sampling modes:

- 1) Baseband **wideband** sampling
- 2) Baseband **preselect** sampling
- 3) **Undersampling**, which is also sometimes called subsampling

To help you get a feel for the filter requirements of each mode, we present a convenient tool for analyzing the effects of sampling in the frequency domain.

Fan-fold Paper Model to Visualize Sampling

- Plot the spectrum of the input signal on transparent fan-fold printer paper scaled so the frequency axis is aligned with multiples of F_s on the backward folds

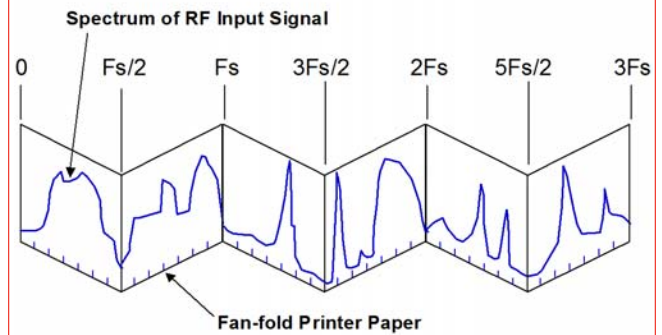


Figure 7

This simple technique has been very useful to our customers and our own applications engineers to help them understand what happens during sampling.

Imagine that we have a stack of the old fan-fold computer printer paper but with transparent sheets.

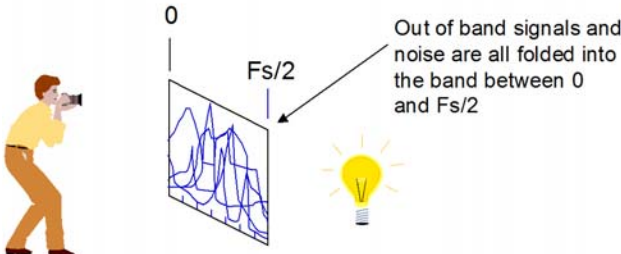
Now, we assign the frequency axis along the bottom edge of this paper, scaled so that multiples of the sampling frequency line up with the backward folds of the paper, as shown.

Using that frequency scale, we plot out the spectrum of the signal we want to sample with amplitude plotted on the vertical axis.

Sampling and Filtering Techniques

Fan-fold Paper Model to Visualize Sampling

- Now collapse the stack of transparent fan-fold paper and look through all the sheets
- This represents how sampling “folds” the entire RF input spectrum into a single page from 0 to $F_s/2$
- Once aliasing occurs, there is no way to undo it



Out of band signals and noise are all folded into the band between 0 and $F_s/2$

Figure 8

Now, let's collapse the stack of transparent paper flat together and hold the stack up to a light so we can see through all the sheets.

We are now looking at the frequency plot of the sampled signal at the output of the A/D converter.

Notice that we've lost a lot of information because we can't tell which sheet a particular signal is on. And, unfortunately, after sampling that information is lost forever.

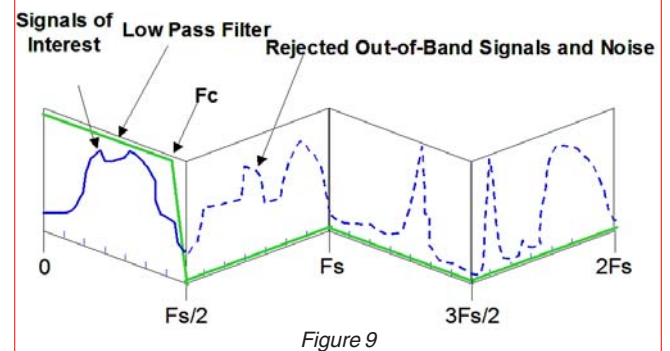
We've also contaminated any particular signal with signals from other sheets which have folded on top of it.

Not only that, we've also folded the noise from all the sheets so they pile up in the region between DC and the half sampling rate, potentially ruining the signal to noise ratio.

How do we avoid this mess in each of the three sampling modes?

Baseband Sampling of Wideband Signals

- For baseband signals over a wide frequency range, use a low pass filter with cutoff frequency, F_c , less than $F_s/2$, where F_s is the A/D sample rate
- After sampling, only the baseband signal is captured, eliminating folding of aliased signals and noise



For the baseband **wideband** sampling mode, where we want to look at everything from DC up to a frequency below the half sampling rate, we can install a low pass filter with a cutoff frequency, F_c , located below $F_s/2$.

The frequency response of the filter is shown in green.

Now, all of the out-of-band signals and noise on the pages above $F_s/2$ are eliminated so that when the folding occurs, it doesn't corrupt the baseband signal.

Sampling and Filtering Techniques

Baseband Sampling of Preselect Signals

- For narrowband signals at baseband, using a pre-select bandpass filter can optimize the dynamic range of the A/D converter by rejecting strong adjacent signals and out-of-band signals and noise
- Pre-select filter is a bandpass filter whose passband is centered on the signal of interest

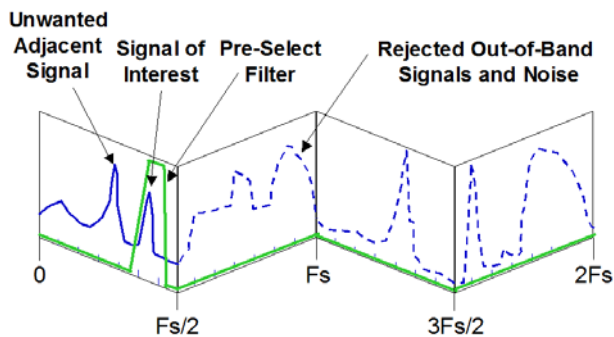


Figure 10

For the baseband **preselect** sampling mode, we need to use a bandpass filter with the frequency response shown in green.

We get the same benefits as the previous case for out-of-band signals and noise above $F_s/2$, but more importantly, we can keep large adjacent signals like the one shown, from getting to the A/D converter.

The reason for this is that if the large unwanted signal gets through to the A/D converter, it uses up its dynamic range.

For applications where there are known, strong unwanted signals, this technique can be extremely useful in improving the signal-to-noise ratio of the smaller signal of interest.

Principles of Undersampling

- For narrowband signals above $F_s/2$, undersampling can be used to intentionally “alias” the input signal
- Very useful for IF outputs of UHF/VHF receivers
- Successful undersampling needs careful selection of:
 - Signal Frequency
 - Signal Bandwidth
 - Bandpass Filter
 - Sampling Frequency

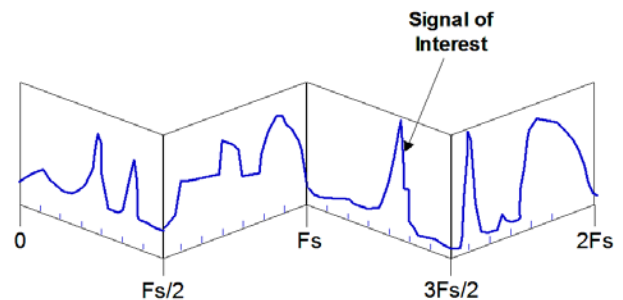


Figure 11

The third sampling mode, called undersampling or subsampling, is ideal for many systems that use an analog RF translator front end. These receivers usually deliver IF outputs, often at 21.4 or 70 MHz, with bandwidths ranging from a few kilohertz to tens of MHz—depending on the receiver.

If we wanted to perform baseband sampling on a 70 MHz signal, we would have to choose a sampling rate of well over 140 MHz. This may require an A/D that adds significant cost and power to the system.

However, because the IF signal is inherently bandlimited, we can take advantage of the folding caused by sampling and use a lower frequency A/D.

This is a little tricky since you have to carefully choose the sampling frequency and filtering according to the signal frequency and bandwidth.

Let's see how.

Sampling and Filtering Techniques

Principles of Undersampling Design: Step 1

- Step 1: Design a bandpass filter or IF filter to pass the band of interest and reject all other signals to meet spurious and S/N requirements
- Tradeoffs
 - Sharper filter adds complexity, expense, calibration, space, etc.
 - Sharper filter allows lower A/D sample rate

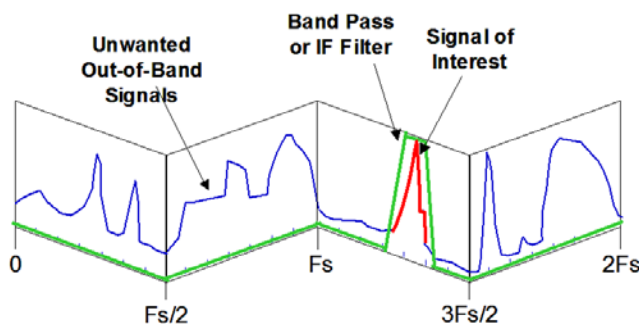


Figure 12

The fan-fold paper really comes in handy here.

First, design a bandpass filter that rejects unwanted signals and noise.

This is often fully satisfied by the standard IF filter in the RF translator, but you do have to check this.

Sharper filters add cost and maintenance but they do let you get away with a lower sampling rate as we'll see in the next figure.

Second (top of next column), choose a sampling frequency so that the passband of the filter, along with its skirts, falls entirely on a single page of fan fold paper.

There are many possible solutions to each case, so you have to pick the one that works best. You may have to go back and forth a few times to readjust the filter and sampling rate to get the best scheme.

Principles of Undersampling Design: Step 2

- Step 2: Choose a sampling frequency so that the filter pass band and skirts fall entirely within one page of the fan-fold paper
- Tradeoffs
 - Higher sampling rate allows broader bandwidth & simpler filter
 - A/D's with lower sampling rates are more accurate & less expensive

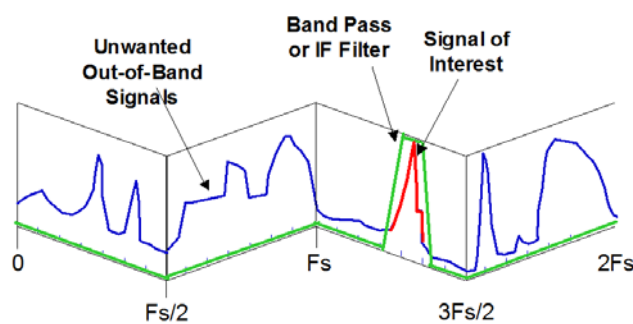


Figure 13

Here are some tradeoffs to consider:

With a higher sampling rate, the pages are wider and the filter becomes less complex. Also, there is a lower noise density folded into the 0 to $F_s/2$ band after sampling.

At higher sampling rates, however, the A/D is more expensive and the number of bits of accuracy drops off.

You also need to be sure that the A/D has a good wideband input stage to handle the IF signal with minimum distortion.

Equally important is the aperture uncertainty or phase jitter of the sample-and-hold amplifier, which is usually part of the A/D.

To make this job easier, many A/D converters are now specifically characterized to operate in undersampling applications.

Sampling and Filtering Techniques

Undersampling Performs Frequency Translation

- Signal of interest folds into the 0 to $F_s/2$ region
- Undersampling performs an automatic frequency translation
- Translated image may be reversed in frequency depending on which side of the “fold” the input falls

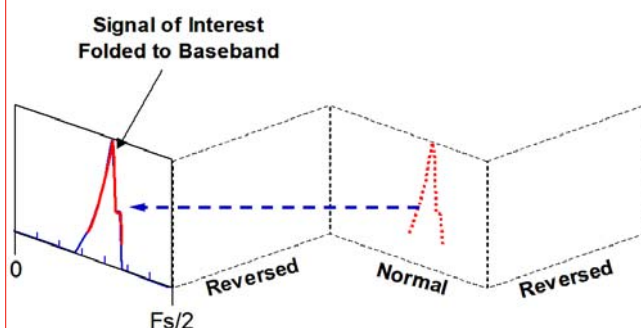


Figure 14

The effect of undersampling, as you probably expected by now, is that the IF signal is folded down to the first page. This is really an automatic frequency translation, performed for free by the sampling process.

For the signals on every odd numbered sheet, the effect is a frequency translation by a multiple of F_s . For the signals on even numbered sheets, there is a reversal of the frequency axis on that sheet, followed by a translation by an odd multiple of $F_s/2$. Again, this is much easier to follow by visualizing the fan-fold model.

This undersampling technique is extremely popular in software radio systems which almost always follow the A/D converter with a DDC (digital downconverter).

Regardless of where the undersampling folding process translated the signal of interest, the DDC can translate it down to 0 Hz as a complex baseband signal. Once the complex signal is at baseband, the reversal of the frequency axis is easily undone by simply changing the sign of the Q component.

Guidelines for Sampling and Undersampling

- Use the fan fold paper to validate your sampling plan for the characteristics of your input signal
- Carefully evaluate A/D specifications for operation in the undersampling mode
- Ensure low-noise, wideband circuitry in the front end ahead of the A/D
- Transforming coupling often is superior to an amplifier for IF or RF input signals
- Eliminate as many out-of-band signals and noise as possible, since they will fold
- Ensure the the sample clock is clean with low phase noise and jitter

Figure 15

There are usually several different sample clock frequencies that will work for undersampling. While the fan-fold paper model can show all of the correct frequency plans, the best choice will usually be determined by several other important practical considerations shown above.

Some A/D converters are specifically characterized for undersampling applications, while others are designed only for baseband sampling. Make sure to verify the specifications.

Noise and distortion of the input signal must be minimized so these components don't fold into the sampled signal. Special care must be taken to preserve the purity of the sample clock signal.

Undersampling can be an extremely valuable tool for software radio applications, since it can eliminate at least one additional stage of analog frequency translation and simplify system design.

Undersampling allows you to use an A/D converter with a lower sampling rate, which usually means more bits of resolution and better dynamic range. This lower sample rate also reduces the cost and complexity of the next stage of digital signal processing, recording, storage, or transmission.

FPGA Technology

FPGAs: The Essential Companion for High Speed A/Ds

- 500+ MHz DSP Slices and Memory Structures
- Over 1000 dedicated on-chip hardware multipliers
- On-board GHz Serial Transceivers
- Partial Reconfigurability Maintains Operation During Changes
- Switched Fabric Interface Engines
- Over 330,000 Logic Cells
- Gigabit Ethernet media access controllers
- On-chip 405 PowerPC RISC micro-controller cores
- Memory densities approaching 15 million bits
- Reduced power with core voltages at 1 volt
- Silicon geometries to 65 nanometers
- High-density BGA and flip-chip packaging
- Over 1200 user I/O pins
- Configurable logic and I/O interface standards



Figure 16

FPGAs, or Field Programmable Gate Arrays, are commonly coupled to high speed A/Ds for two key reasons:

- They can perform real-time digital signal processing faster than general purpose programmable processors
- They offer extremely high speed interfaces to other system components including built-in interfaces to high-speed switched serial fabrics.

BGA and flip chip packages provide plenty of I/O pins to support these on-board gigabit serial transceivers and other user-configurable system interfaces.

Other important features are on-chip processor cores, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

Dedicated hardware multipliers started appearing a few years ago and now you'll find literally hundreds of them on chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from silicon geometries shrinking down to 0.1 microns.

FPGAs: New Development Tools

- High Level Design Tools
 - Block Diagram System Generators
 - Schematic Processors
 - High-level language compilers for VHDL & Verilog
 - Advanced simulation tools for modeling speed, propagation delays, skew and board layout
 - Faster compilers and simulators save time
 - Graphically-oriented debugging tools
- IP (Intellectual Property) Cores
 - FPGA vendors offer both free and licensed cores
 - FPGA vendors promote third party core vendors
 - Wide range of IP cores available



Figure 17

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer many application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.

FPGA Technology

FPGAs: Key Resources for DSP

- Parallel Processing
- Hardware Multipliers for DSP
 - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
 - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
 - Systolic simultaneous data movement
- Flexible I/O
 - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions



Figure 18

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 500 of them on a single FPGA.

This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.

FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.

These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.

Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

As we said, FPGAs now have specialized serial and parallel interfaces to match requirements for high-speed peripherals and buses.

FPGAs Bridge the SDR Application Task Space

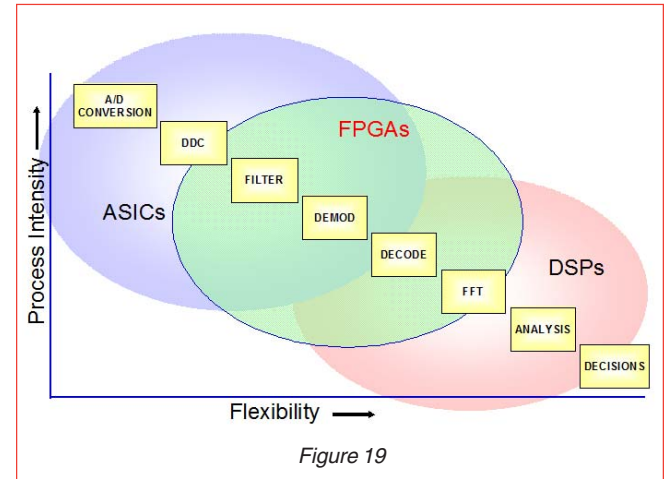


Figure 19

As a result, FPGAs have significantly invaded the application task space as shown by the center bubble in the task diagram above.

They offer the advantages of parallel hardware to handle some of the high process intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.

These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the performance and capabilities of these remarkable devices.

FPGA Technology

FPGA Resource Comparison

	Virtex-II Pro VP50, VP70	Virtex-4 FX, LX, SX	Virtex-5 FXT, LXT, SXT	Virtex-6 LXT, SXT
Logic Cells	53K–74K	41K–152K	46K–156K	128K–476K
Slices*	24K–33K	18K–68K	7K–24K	20K–74K
CLB Flip-Flops	47K–66K	49K–93K	150K–207K	160K–595K
Block RAM (kb)	4,176–5,904	1,728–6,768	2,160–8,784	9,504–38,304
DSP Hard IP	18x18 Multipliers	DSP48	DSP48E	DSP48E
DSP Slices	132–328	64–512	48–640	480–2,016
Serial Gbit Transceivers	–	0–20	12–16	20
PCI Express Blocks	–	–	–	2
SelectIO	–	448–768	480–640	600

*Virtex-II Pro and Virtex-4 Slices actually require 2.25 Logic Cells;
 Virtex-5 and Virtex-6 Slices actually require 6.4 Logic Cells

Figure 20

The above chart compares the available resources in the four Xilinx FPGA families that are used in most of the Pentek products.

- Virtex-II Pro: VP50 and VP70
- Virtex-4: FX, LX and SX
- Virtex-5: FXT, LXT and SXT
- Virtex-6: LXT and SXT

The Virtex-II family includes hardware multipliers that support digital filters, averagers, demodulators and FFTs—a major benefit for software radio signal processing. The Virtex-II Pro family dramatically increased the number of hardware multipliers and also added embedded PowerPC microcontrollers.

The Virtex-4 family is offered as three subfamilies that dramatically boost clock speeds and reduce power dissipation over previous generations.

The Virtex-4 LX family delivers maximum logic and I/O pins while the SX family boasts of 512 DSP slices for maximum DSP performance. The FX family is a generous mix of all resources and is the only family to offer RocketIO, PowerPC cores, and the newly added gigabit Ethernet ports.

The Virtex-5 family LXT devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SXT devices push DSP capabilities with all of the same extras as the LXT. The FXT devices follow as the embedded system resource devices.

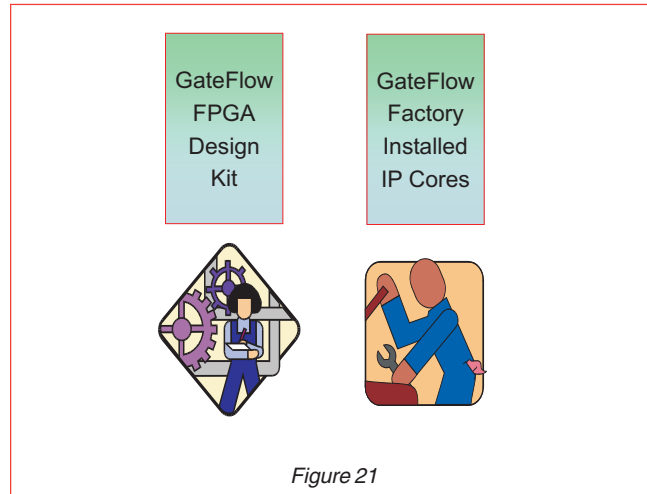
The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 devices offer higher density, more processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements including PCI Express. Virtex-6 supports PCI Express 2.0 in x1 through x8 configurations.

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 family. Increases in operating speed from 500 MHz in V-4 to 550 MHz in V-5 to 600 MHz in V-6 and increasing density allows more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 2016 DSP slices.

FPGA Technology

Pentek GateFlow FPGA Design Resources



GateFlow® is Pentek's flagship collection of FPGA Design Resources. The GateFlow line is compatible with the Xilinx Virtex products and is available as two separate offerings:

If you want to add your own custom algorithms, we offer the GateFlow FPGA Design Kit.

We also offer popular high-performance signal-processing algorithms with the GateFlow factory-installed IP Cores. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products

Installed Cores are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully supported with Pentek ReadyFlow® Board Support Packages.

Let's start with the GateFlow FPGA Design Kit.



GateFlow FPGA Design Kit

- Allows FPGA design engineers to easily add functions to standard factory configuration
- Includes VHDL source code for all standard functions:
 - Control and status registers
 - A/D and Digital receiver interfaces
 - Mezzanine interfaces
 - Triggering, clocking, sync and gating functions
 - Data packing and formatting
 - Channel selection
 - A/D / Receiver multiplexing
 - Interrupt generation
 - Data tagging and channel ID
- **User Block** for inserting custom code



Figure 22

If you want to add your own algorithms to Pentek catalog products, we offer the GateFlow FPGA Design Kit that includes VHDL source code for all the standard factory functions.

VHDL is one of the most popular languages used in the FPGA design tools. The GateFlow Design Kit includes the VHDL source code for every software module we use to create these standard factory features of the product.

The standard factory configuration supports a wide range of operating modes, timing and sync functions, as well as several different data formatting options.

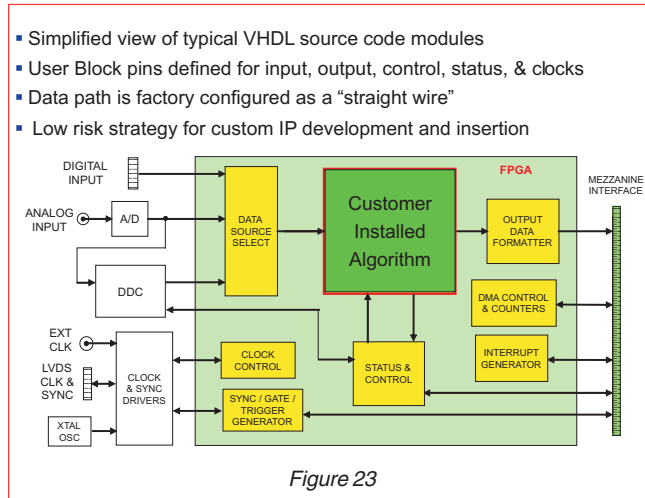
This includes control and status registers, peripheral interfaces, mezzanine interfaces, timing functions, data formatting, channel selection, interrupt support, and data tagging.

These are also fully supported with our ReadyFlow Board Support Package.

We also include a special User Block, positioned right in the data stream, so you can easily drop in your own custom signal processing algorithms.

FPGA Technology

GateFlow Design Kit User Block



Here's a simplified block diagram of a typical software radio module showing the FPGA as the large green box and external hardware devices connected to it.

The yellow blocks inside the FPGA are VHDL code modules that handle the standard factory functions and interfaces.

The User Block is a VHDL module that sits in the data path with pin definitions for input, output, status, control and clocks.

In the standard product, the User Block is configured as a straight wire between input and output.

If the FPGA designer can create an IP core or a custom algorithm inside the User Block so that it conforms to the pin definition, he will have a very low-risk experience in recompiling and installing his custom code.

And remember, he can also make changes outside the User Block, since we provide source code for all the modules.

GateFlow Design Kit Project Files

- Project files for Xilinx Foundation ISE Tools
 - Archived project files for default factory configuration for standard factory product operation
 - VHDL source code for all project files
 - Software module interconnect block diagram
 - JTAG chain definition files
 - User Block I/O connections diagram
- Complete Pentek Project Directory
 - Ready to start development
- Other files
 - Pentek FPGA Design Kit User's Manual
 - FPGA manufacturers data sheet and user's guide
- FPGA Loader Utility



Figure 24

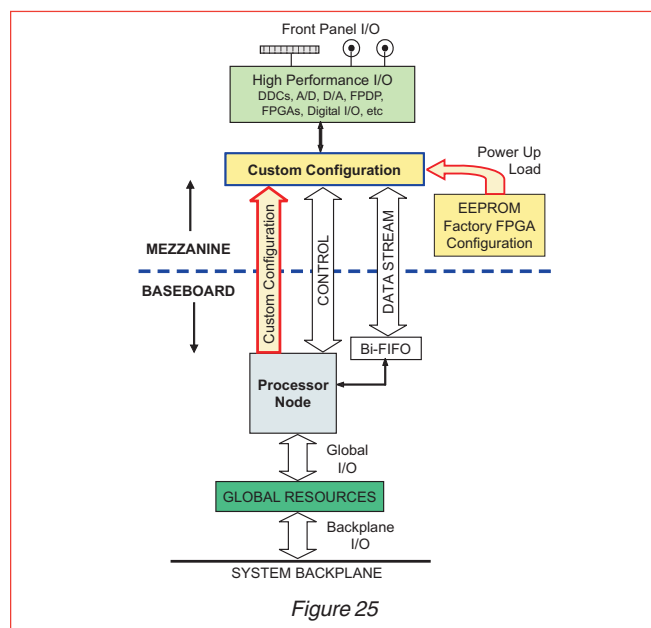
The GateFlow Design Kit is intended to be used with the Xilinx ISE Foundation Tool Suite. Customers should be trained and familiar with this tool and FPGA design principles, in general.

The design kit installs as a complete project file within the ISE environment and includes all of the project files that Pentek engineers used to create the standard factory product. These include configuration and definition files, VHDL source, JTAG definition files, and I/O block diagrams.

The design kit also includes several utilities, but one important resource is the FPGA Loader Utility.

FPGA Technology

GateFlow Design Kit FPGA Loader Utility



Normally, the FPGA is loaded from a nonvolatile EEPROM with the standard factory configuration code, when the product is powered up.

The FPGA Loader Utility allows the processor associated with the FPGA product to reconfigure the FPGA as a software task, effectively overwriting the factory configuration code.

This can be done without turning off power, without disassembling the board or system and without attaching any special cables or harnesses to the board.

In this way, the FPGA can be reconfigured during initialization to install custom operational modes and features. It can also facilitate product upgrades and enhancements to dramatically extend product longevity.

The Loader Utility is especially useful as a runtime resource. The user can select a new mode of operation and cause a new FPGA configuration upload, to implement that mode as part of the runtime executable code.

GateFlow Installed IP Cores

- Pentek Installs IP Cores in Pentek Products
- Cores are tailored and optimized for:
 - Specific devices and I/O found on Pentek products
 - Efficient FPGA resource utilization
 - Execution and throughput speed
- Eliminates need for customer FPGA development
- Fully supported with ReadyFlow Board Support Libraries

Figure 26

Pentek is an AllianceCore Member, a third party program sponsored by Xilinx for companies that specialize in specific areas of expertise in developing FPGA algorithms for niche application areas. These include image processing, communications, telecom, telemetry, signal intelligence, wireless communications, wireless networking, and many other disciplines.

Pentek offers popular high-performance signal processing algorithms installed in Pentek products. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products. The cores take full advantage of the numerous hardware multipliers to achieve highly-parallel processing structures that can dramatically outperform programmable RISC and DSP processors.

Installed Cores are optimized for efficient FPGA resource utilization, execution and throughput speed. They are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully tested and supported with the Pentek ReadyFlow Board Support Packages. Purchasing these popular factory-installed cores saves you the time and costs of acquiring FPGA tools and developing custom FPGA code.

Switched Serial Fabrics

Switched Serial Gigabit Interfaces - Why?

- Too many different I/O technologies per system
 - FPDP, PCI, VME, Ethernet, RS-232, FibreChannel, SCSI, PMC, IP, 1553, LVDS, ATM, etc.
- Bus backplanes are major data bottlenecks
 - All boards must share a common bus, one at a time!
- Parallel switched fabrics are expensive
 - RACEway was controlled by one vendor
- Cabling increases system cost and complicates maintenance
 - Cables and connectors can be a major factor in MTBF
- Software upgrades are difficult for specialized interfaces
 - Performance goals require software tuning of signal paths
- Need a better solution for moving data !
 - Fast, flexible, open, and inexpensive



Figure 17

The VMEbus still serves as the dominant bus structure for high-performance real-time embedded systems. As requirements grew following its introduction, VME acquired new interfaces such as VSB, RACEway, RACE++, VME64 et al. that provided improved performance.

All these different I/O technologies caused new problems with backplanes creating data bottlenecks and interfaces controlled by one vendor. System costs increased due to cabling, maintenance and software upgrades. A better solution for moving data was needed and it had to be fast, flexible, and inexpensive.

The answer turned out to be Switched Serial Gigabit Interfaces.

High-Speed Switched Serial Interfaces

- Gigabit serial links send data over a pair of wires using differential signaling
- Sequential 1s and 0s are sent over the pair of wires at a fixed bit rate
 - Popular serial rates: 10 MHz, 100 MHz, 1 GHz, 2.5 GHz, 3.125 GHz, etc.
- The clock, data, and data word framing are encoded into the serial bits stream, typically using 8B10B coding:
 - 10 bits of serial transmission are required to deliver 8 bits of data
 - Extra 2 bits maintain synchronization, framing and DC line balance
- SERDES - Serializer / Deserializer
 - Serializer: Encodes clock, frame, and 8 bits of data into a 10-bit stream
 - Deserializer: Decodes clock, frame and 8 bits of data from a 10-bit stream
 - Usually combined into one device for full duplex operation

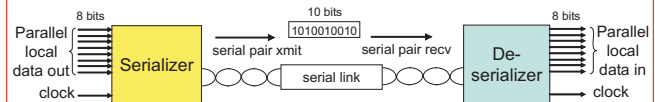


Figure 28

A switched serial fabric system connects devices together to support multiple simultaneous data transfers, usually implemented with a crossbar switch. Using differential signaling, data is sent over a pair of wires at a fixed bit rate such as 100 MHz, 1 GHz, 2.5 GHz, 3.125 GHz, etc.

The clock, data, and data word framing are encoded into the serial stream, usually with 8B10B coding: ten bits of serial transmission deliver eight bits of data. The extra two bits maintain synchronization, framing and DC line balance.

The Serializer shown in Figure 2 encodes clock, frame, and eight bits of data into a 10-bit stream. The Deserializer decodes the 10-bit stream into clock, frame, and eight bits of data. These two functions are usually combined into one device for full duplex operation, known as the SERDES (SERializer/DESerializer).

Switched Serial Fabrics

Gigabit Serial Data Rates

■ Gigabit Serial Data Transfer Rates Depend On:

- Serial clock frequency (serial bit rate)
- Number of bit "lanes" ganged together (e.g., 4X = 4 bit lanes)
- Physical layer encoding overhead (8B10B): 80% Efficiency
- Peak Rate (MB/sec) = (Serial Rate x Lanes x 80%) ÷ (8 bits per byte)

$$= (\text{Serial Rate} \times \text{Lanes}) \div 10$$

Bit Clock	Peak Rates for Specified Number of Bit Lanes		
	1X	4X	8X
1 GHz	100 MB/sec	400 MB/sec	800 MB/sec
2.5 GHz	250 MB/sec	1 GB/sec	2 GB/sec
3.125 GHz	312 MB/sec	1.25 GB/sec	2.5 GB/sec

Figure 29

The raw speed of serial fabrics is governed by three factors:

The serial bit clock frequency; the inherent 8B10B channel encoding efficiency of 80%; and the number of lanes or parallel bit streams ganged together in the interface.

Since there are 8 bits per byte, the peak rate expressed in MB/sec becomes the serial rate expressed in GHz, times the number of lanes, divided by 10.

For VXS, with four bit lanes or 4X, the peak transfer rate in each direction is the serial bit clock divided by 2.5.

The table above shows the transfer rates for each VXS link for 1, 2.5, and 3.125 GHz bit clocks.

Of course, there is some additional overhead in the packet protocols, some of which are presented next.

Popular Gigabit Serial Protocols

- Too many different I/O technologies per system
 - FPDP, PCI, VME, Ethernet, RS-232, FibreChannel, SCSI, PMC, IP, 1553, LVDS, ATM, etc.
- Bus backplanes are major data bottlenecks
 - All boards must share a common bus, one at a time!
- Parallel switched fabrics are expensive
 - RACEway was controlled by one vendor
- Cabling increases system cost and complicates maintenance
 - Cables and connectors can be a major factor in MTBF
- Software upgrades are difficult for specialized interfaces
 - Performance goals require software tuning of signal paths
- Need a better solution for moving data !
 - Fast, flexible, open, and inexpensive

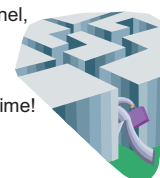


Figure 30

Xilinx offers a simple link layer protocol IP core engine called Aurora that interfaces with the RocketIO gigabit serial physical layer interfaces available in the Virtex-II Pro family.

Altera supports its Stratix GX Multi-Gigabit Transceivers with the SerialLite link layer protocol as well as full implementations of switched fabric IP cores.

The nice thing about this strategy is that you can design and build FPGA-based hardware products that adapt to different fabrics, depending on the protocol IP core you install.

VITA 49 is a radio transport protocol for SDR (Software Defined Radio) architectures that enables interoperability between diverse SDR components from different vendors

PCI Express is Intel's initiative for connectivity between processors and boards in personal computers and workstations. It's been used extensively to improve performance of graphics boards in Vista computers.

RapidIO is a packet-switched fabric targeted for embedded computer component vendors and system integrators. It addresses the needs of real-time computing at several levels.

Switched Serial Fabrics

Dedicated Point-to-Point Serial Links

■ Dedicated Hardwired Connections

- Paths are based on particular application requirements
- Paths set up during system integration with cables or fixed wiring
- Applications: Aurora, VITA 49, PCI Express, Serial RapidIO

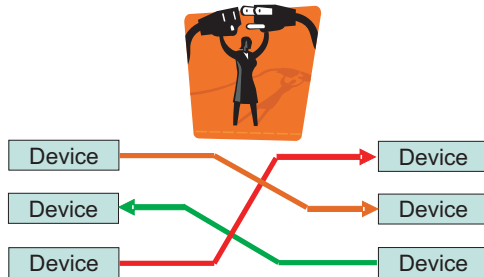


Figure 31

The first type of serial links is the dedicated point-to-point link. As its name implies, it utilizes dedicated hardware connections and its paths are based on the requirements of the particular application. The paths are set up during system integration and utilize cables or fixed wiring.

Applications that utilize dedicated point-to-point serial links include those that are running Aurora, VITA 49, PCI Express and RapidIO.

Manually-Switched Point-to-Point Links

■ Software Configurable “Protocol Transparent” Switch

- Switch paths are changed in hardware “manually” by a control processor
- Paths can be changed during initialization and during runtime
- Switch is transparent to the serial protocol
- Switch supports virtually all gigabit serial links
- Applications: Aurora, VITA 49, PCI Express, Serial RapidIO
- Switching Scheme for Pentek 4207

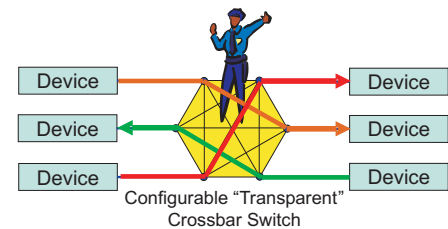


Figure 32

Next in line are manually-switched point-to-point serial links. Think of them as “protocol transparent” switches that are software configurable. In this case the switch paths are changed in the hardware “manually” by a control processor that directs the traffic. They can be changed during system initialization and during runtime.

This switch supports virtually all gigabit serial links and it’s transparent to the serial protocol. It can be used in applications running Aurora, VITA 49, PCI Express and Serial Rapid IO.

This type of switch is used In the Pentek Model 4207 PowerPC I/O Processor. More about this VME/VXS board in the Products and Applications sections.

Switched Serial Fabrics

Memory-Mapped Serial Links

- One system processor establishes memory map for all devices
 - This function is known as the “root complex”
- Switches or bridges implement defined memory mapped connections
- Supports multiple “initiators” and multiple “targets”
- Arbitration is done through token passing
- Does not provide automatic re-routing
- Example: PCI Express

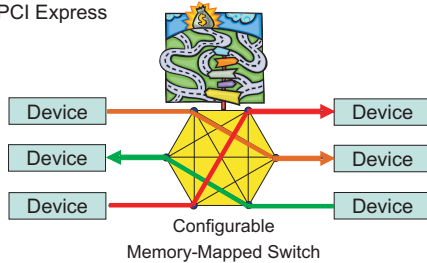


Figure 33

Memory-mapped serial links are based on a memory map that's established by a system processor.

The defined memory-mapped connections are implemented with hardware switches or bridges.

This type of link supports multiple “initiators” and multiple “targets”. Arbitration is done through token passing and automatic-rerouting is not supported.

A protocol example that uses this link is PCI Express.

Packet-Switched Serial Links

- Switched “fabric” protocol uses data packets that include:
 - Header information to identify source, destination, packet type, data size, time stamp, sequence number, and priority
 - Data “payload”
 - Footer information for checksum and end of packet marker
- Intelligent switch evaluates packet header to determine routing
- Automatic re-routing through alternate switch paths avoid conflicts
- Packets and Switch are unique and dedicated to a particular protocol
- Supports multiple processors
- Example: Serial RapidIO

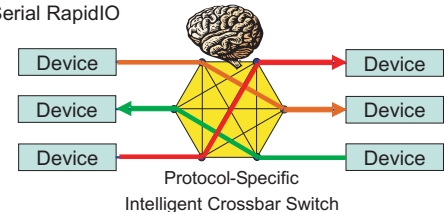


Figure 34

Packet-switched serial links utilize a switched fabric protocol that uses data packets. Each data packet includes:

- A header that provides information to identify the source, destination, packet type, data size, time stamp, sequence number and priority
- The data “payload” which contains the actual data
- A footer with checksum and end of packet marker information

This intelligent switch evaluates packet header information to determine the routing. Automatic rerouting through alternate paths avoids conflicts. The packets and the switch support multiple processors. They are unique and dedicated to a particular protocol

Applications running Serial RapidIO can utilize this packet-switched fabric.

Switched Serial Fabrics

Comparison of Serial Links

	 Dedicated Point-to-Point	 Manually Switched Point-to-Point	 Memory Mapped Fabric	 Packet Switched Fabric
Software Reconfigurable Paths	No	Yes	Yes	Yes
Self-Routing Packets	No	No	No	Yes
Automatic Path Re-Routing	No	No	No	Yes
Packet Overhead Required	Low	Low	Med	High
Payload Data Efficiency	High	High	Med	Low
Software Driver Complexity	Low	Low	Med	High
FPGA Interface Complexity	Low	Low	Med	High
Protocol Transparent	Yes	Yes	No	No
Protocols Supported	Aurora VITA 49 PCIe SRIO	Aurora VITA 49 PCIe SRIO	PCIe	SRIO

Figure 35

This table provides a side-by-side comparison of the four types of serial links we discussed in the previous pages and summarizes their main properties and supported protocols.

It can help the system designer narrow down the available links and protocols when evaluating the requirements of a proposed high-speed embedded system.

Switched Serial Fabrics

VXS: Switched Serial Fabric for VME

- VITA 41 Specification for 6U VMEbus
- Two Card Types Defined: Payload and Switch
- Payload Card
 - Processor, DSP, Memory, I/O, A/D, D/A, etc
 - Two 4x Serial Switched Fabric Ports on New P0 Connector
- Switch Card
 - Serial Fabric Crosspoint Switch
 - Joins Payload Cards via Backplane Wiring
- Base VITA 41.0 defines mechanical & electrical details
 - Completely independent of any serial protocol
- Protocol implementations are defined in sub-specifications

Figure 36

VXS: Specification Status

- VITA Standards Organization
 - Develops and maintains VXS Specification
- VITA 41.0
 - VXS Base Specification Released
 - General info, mechanicals, connector, etc
- VXS Sub-specifications

• VITA 41.1	Infiniband Protocol Layer	Released
• VITA 41.2	Serial RapidIO Protocol Layer	Released
• VITA 41.3	Gigabit Ethernet	Working Group
• VITA 41.4	PCI Express	Working Group
• VITA 41.6	Gig-Ethernet Control Plane	Working Group
• VITA 41.10	Live Insertion	Working Group
• VITA 41.11	Rear Transition Modules	Working Group

Figure 37

VXS is the popular name for a switched serial backplane fabric implementation for VMEbus.

Officially, it is being defined by the VITA standards organization as specification VITA 41. It defines two types of cards.

The VXS Payload Card is a processor, memory or I/O board, identical in concept to popular board functions already in use.

It has a new P0 connector that contains two 4X serial ports for data transfers across the backplane.

Each 4X serial port has four differential gigabit serial lines ganged together for input and another four serial lines for output, and they are commonly referred to as 4X serial ports.

Serial bit rates on each line are defined for frequencies up to 10 gigabits/second.

The VXS Switch Card is a new type of board with many serial ports and cross point switches to join the Payload cards.

The VXS specification is fabric-transparent, in that there are subspecifications, one for each of five fabrics.

As of this writing, the base specification that contains general information and the mechanical and connector specs has been released.

Two protocols, the Infiniband and the Serial RapidIO have also been released.

Three additional protocols are being developed by the VITA 41 Working Group. This group is also working on the live insertion spec and rear transition modules.

Switched Serial Fabrics

VXS Payload Card

- Typical functions: processor, CPU, memory, I/O
- Mechanically compatible with legacy VME boards
- Uses standard VME64x connector for P1 & P2
- Uses new MultiGig RT2 serial connector (between P1 & P2)
- Two Full-Duplex 4X Serial Ports: 1.25 GBytes/sec each

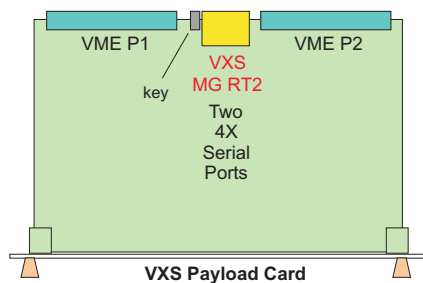


Figure 38

The VXS Payload card has a standard 6U VME outline with standard VME64x backplane connectors for P1 and P2.

You can see the new P0 backplane connector mounted between P1 and P2.

This is the new seven row MultiGig RT-2 connector for P0 and it handles two full duplex 4X serial ports.

VXS Switch Card

- Uses 6U VME board size
- No connection to VMEbus – instead five multiGig RT2
- Up to eighteen 4X serial ports to join VXS payload cards
- Up to four 4X serial ports to join other VXS switch cards
- Special backplane power connector and keying
- VXS backplane joins switch and payload boards

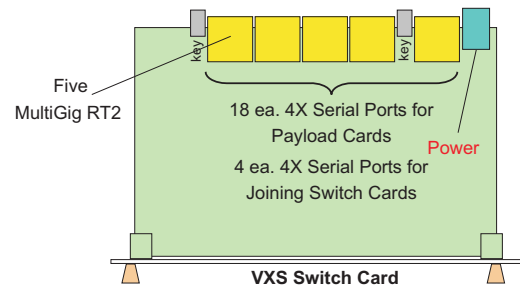


Figure 39

The VXS Switch card has a 6U VME board form factor but no P1 and P2 connectors.

Instead, it uses several MultiGig RT-2 connectors to handle up to eighteen 4X full-duplex switched serial ports.

This board joins the payload cards so they can talk to each other.

As you may already have guessed, we obviously need a new backplane.

Switched Serial Fabrics

Example: VXS Switch Card

- Connects to payload cards (18) and other switch cards (4)
 - Switch may be manual “fabric transparent” or automatic “protocol specific”
 - Optional links to copper or optical interfaces to networks or other chassis
- Switch cards may have any number of ports

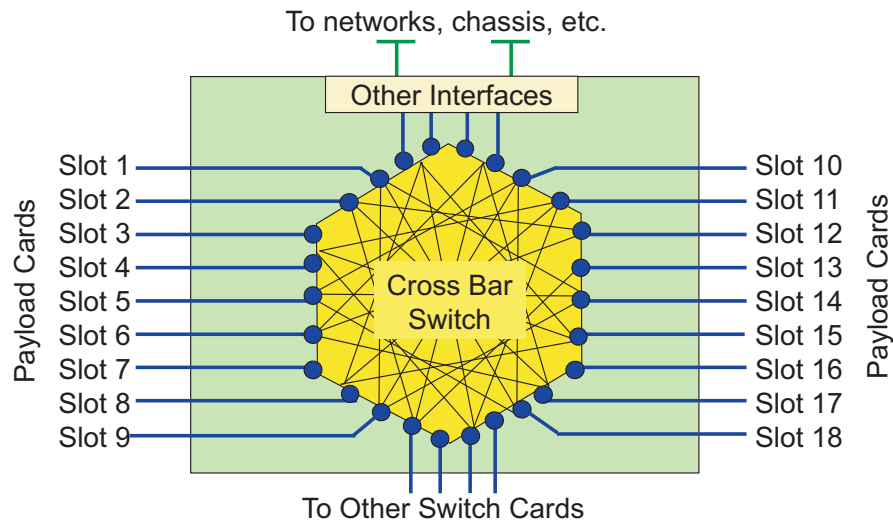


Figure 40

Looking inside just one example of a VXS switch card, we see a big cross point switch for handling traffic between payload boards.

We also see possible front panel connections to other interfaces like networks or storage devices.

With this architecture, any of the five fabrics can be used to deliver an incredibly well-connected solution for high-performance embedded systems.

Switched Serial Fabrics

Example: 20-slot VXS Dual Redundant Backplane

- MultiGig RT2 sockets are used for two 4X serial links
- One or two switch cards occupy special central slot(s)
- 4X links join every payload card to every other payload card via two paths

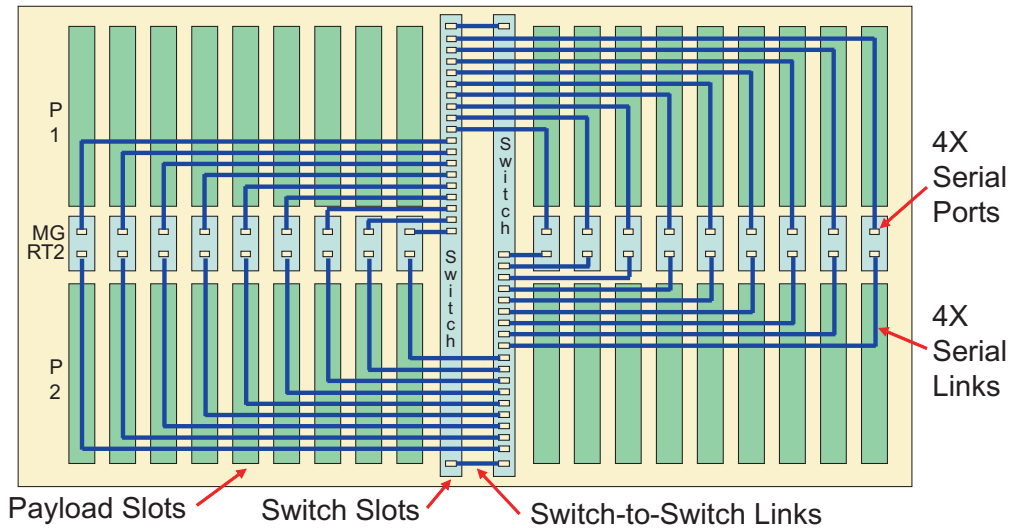


Figure 41

Here's a possible implementation of a 20-slot VXS backplane.

It has 18 payload slots, nine on the left and nine on the right. It also has two switch slots in the center.

The P0 connectors on the payload boards each have two 4X serial ports that are wired in copper through the backplane to the 4X serial ports on the switch boards.

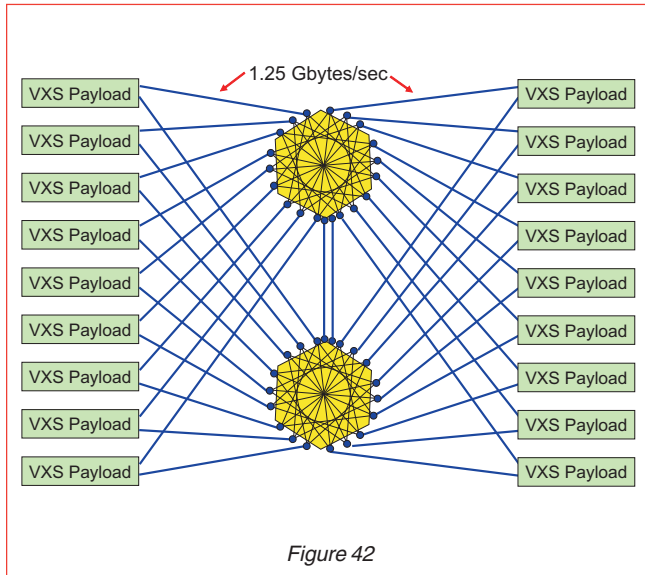
Notice there are two links between the switch boards so they can talk to each other as well.

This arrangement gives you two redundant serial links between every pair of boards in the cage.

And remember, unlike a bused backplane, all of these switched links can be operating at the same time.

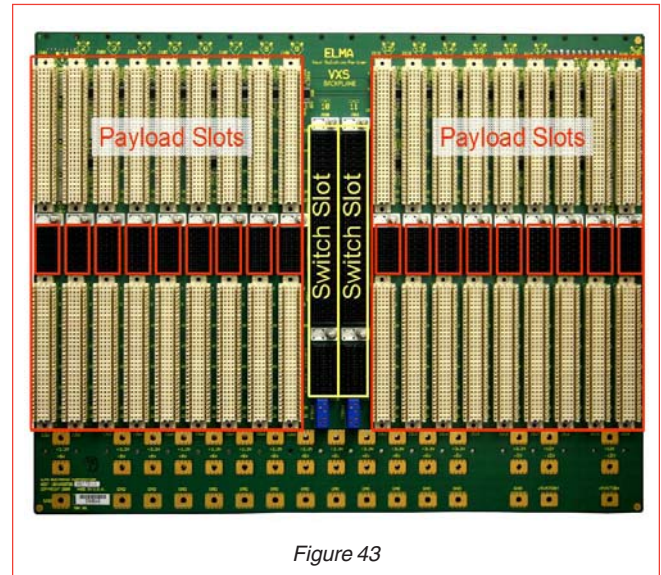
Switched Serial Fabrics

Example: 20-Slot VXS Dual Redundant Backplane



This diagram shows how the 18 payload cards connect to each switch card in the 20-slot backplane.

All 1.25 Gbytes/sec serial links are operating at the same time.



This is a photograph of the commercially available 20-slot VXS backplane with 18 payload cards and two switch cards.

Switched Serial Fabrics

XMC: Switched Serial Fabric for PMC

VITA Doc	Description	Status
42.0	Base Specification, general info, Released connectors, mechanical, etc.	Released
42.1	Parallel RapidIO	Released
42.2	Serial RapidIO	Released
42.3	PCI Express	Released
42.4	HyperTransport	Working Group

Figure 44

Defined under VITA 42, the XMC specification extends the PMC card by adding new connections to support gigabit serial interfaces plus a growing list of alternative I/O standards.

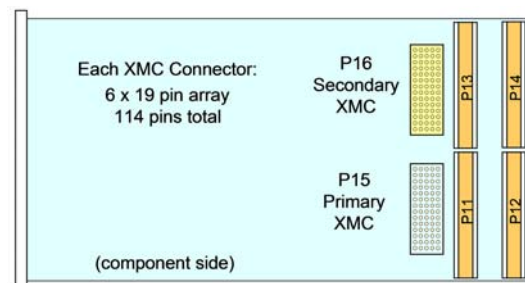
As shown in Figure 44, VITA 42.0 is the base specification that includes general information, reference and inheritance documentation, dimensional specifications, connectors, pin numbering and primary allocation of pairing and grouping of pin functions.

XMCs can be single- or double-width modules that use a pin-socket connector with 114 pins arranged in a 6 x 19 array. A single-width XMC can have one or two connectors with pin functions as shown in Figure 19. A double-width XMC can have up to four connectors.

To support gigabit serial interfaces, notice that both P15 and P16 connectors define 10 full-duplex differential pair lines. The VITA 42.0 base specification does not dictate signal types, data rates, protocols, voltage levels or grouping for these signals. Instead, it wisely leaves that up to the several subspecifications that follow, allowing XMCs to evolve as new standards emerge.

In fact, contrary to the fundamental mission of supporting serial interfaces, the first subspecification, VITA 42.1, defines these same pins for Parallel RapidIO. While VITA 42.1 is approved and fielded, few vendors have embraced this standard and have instead opted for the more popular serial protocols.

PMC/XMC Connector Definition



P15 Primary XMC Connector

- 10 differential pairs each direction
- JTAG
- System Management
- Auxiliary
- 3.3 V Power:
 - Main: 4 pins, 1 A/pin, 13.2 W
 - Auxiliary: 1 pin, for system management
- Variable Power
 - 8 pins, 1 A/pin
 - 5 V (40 W max) or 12 V (96 W max)
 - Modules must accept 5 V or 12 V
 - Carriers may provide 5 V or 12 V

P16: Secondary XMC Connector

- 10 more differential pairs each direction
- High-speed or single-ended user I/O
- Extensions of gigabit serial fabrics

Figure 45

As shown in Figure 45, most of the pins on P15 are reserved for serial links, power and other functions, but P16 has a wealth of user-defined pins now being addressed by the VITA 42.10 General Purpose I/O draft specification. It offers a standardized way of implementing interfaces for popular system I/O including Ethernet, USB ports, RS-232, RS-485, Serial ATA, Fibre Channel, and SAS (Serial Attached SCSI). The clear benefit here is that by following these definitions, XMC and carrier board designers can achieve a much wider range of interoperability, the essential goal of industry standards.

Switched Serial Fabrics

5-Slot Switchless VXS Backplane

- Pentek and Bustronic
 - Division of Elma, Fremont, CA
 - Joint development effort
- Three VXS Slots
 - Two 4X serial links per VXS slot
 - All 4X ports are joined in a ring
 - Each card connects to the other two
- Objectives
 - Requires no VXS Switch Card
 - Low cost VXS development platform
 - Ideal production test platform
 - Supports simple VXS systems

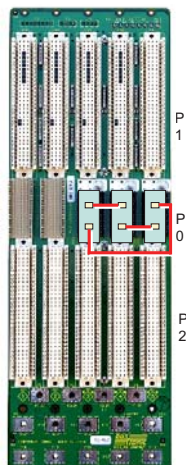


Figure 46

Bustronic and Pentek jointly developed a simple, 5-slot VXS backplane that allows developers to get started with VXS technology without the need for a VXS switch card.

The backplane has three VXS payload slots and two legacy VME slots. All five slots share the common VMEbus.

Since there is no VXS switch card slot, the two 4X VXS links of each of the three VXS payload cards are joined together in a ring.

Each VXS card connects to the other two VXS cards through one dedicated 4X serial link capable of operating any protocol, including the Xilinx Aurora link layer protocol.

One benefit of this backplane is that it provides a low-cost development and product test platform for board vendors. It also provides system integrators with a low-cost platform for smaller systems with just a few cards that need extremely high-speed interconnects between the cards.

Switchless Backplane System

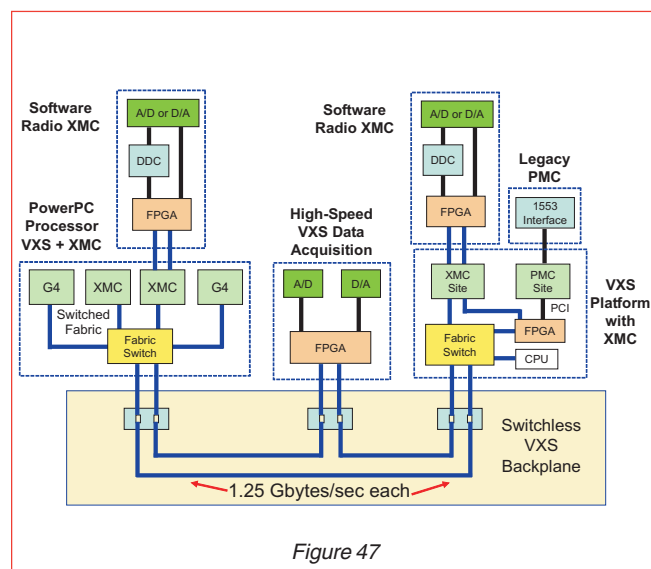


Figure 47

The system above, based on the switchless 5-slot VXS backplane, shows a PowerPC VXS board connected to a high-speed data acquisition VXS board and a VXS platform with both XMC and PMC module sites.

The PowerPC board has a software radio XMC module connected to its XMC site. The VXS platform has also an XMC software radio connected to its XMC module site and a legacy 1553 board connected to its PMC module site.

Each of the VXS link connections shown provides a full-duplex data path operating at speeds up to 1.25 GB/sec each.

Switched Serial Fabrics

VPX: VXS on Steroids

- Improves Number of Switched Fabric Ports over VXS
 - VXS uses only one MultiGig RT Connector – 2 gigabit serial 4x ports
 - VPX uses 3 to 7 MultiGig RT Connectors – 8 to 24 gigabit serial 4x ports
- Optional Switch Card
 - Most payload cards have switches on board
- 3U and 6U VME board form factors
 - IEEE 1101.1 and 1101.2
- Improves I/O Capacity
 - VME front panel I/O is restricted in military systems
 - Migrates to backplane connections for I/O
- Modernizes Power Distribution
 - Uses higher voltage on backplane with on-board power supplies
- Utilizes XMC Mezzanines
 - Maintains VITA 42 XMC Specification

Figure 48

By extending the use of gigabit serial links already proven under VXS, the embedded community created the VPX initiative, which was formally defined under VITA 46. As a migration from the earlier VME and VXS standards, VPX shares the same outline as 3U and 6U cards and supports XMC mezzanine modules defined under the VITA 42 standard.

While VXS allows only one MultiGig RTS connector on a 6U card, VPX extends that number to three for a 3U card and to seven for a 6U card. As a result, VPX payload cards support a much higher traffic bandwidth than VXS, with eight to 24 gigabit serial 4X ports compared to only two with VXS.

Like the VXS specification, the VITA 46.0 VPX base specification does not define backplane topologies or specific gigabit serial fabrics or protocols. As with VXS, implementations of each fabric protocol are defined as sub specifications, or “dot specs.”



VPX REDI

- REDI - Ruggedized Enhanced Design Implementation
- Defines Specific Mechanical Design Implementations for VPX
- Enhanced thermal management
 - Air, conduction, and liquid cooling
- Improved structural integrity
 - Cover plates to protect circuitry and ESD protection
- 2 Level Maintenance compatibility
 - Modules can be field swapped for field maintenance
- Dot Specifications Define Implementation Details
 - VITA 48.1 – REDI Air Cooling
 - VITA 48.2 – REDI Conduction Cooling
 - VITA 48.3 – REDI Liquid Cooling
 - VITA 48.5 – Air Flow Through Cooling

Figure 49

As industry started using VPX, a new extension emerged to deal with severe environmental requirements. The VITA 48 REDI (Ruggedized Enhanced Design Implementation) defines specific mechanical designs for enhanced thermal management using forced air, conduction cooling, and liquid cooling methods. It also defines protective metal covers for the cards to satisfy new requirements for simplified field servicing in deployed military applications.



Switched Serial Fabrics

3U VPX Board

- 3U board outline same as 3U VME
- P0 Utility Connector
 - Power, system reset, reference clock, bus management, addressing, etc.
- MultiGig RT-2 for P1 and P2 Signal Connectors
 - Definitions for differential or single-ended signals
 - Up to eight 4X gigabit serial ports
- One XMC mezzanine site

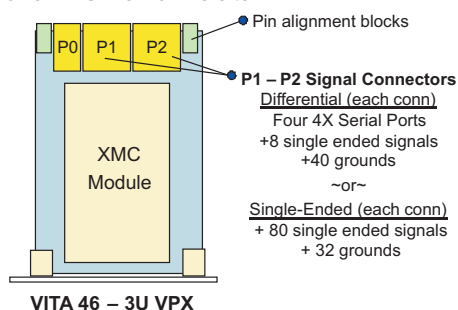


Figure 50

The 3U board outline is the same as the 3U VME board. The board has a P0 Utility connector which provides power, system reset, reference clock, addressing, bus management, and any other required utility functions.

The 3U board has two MultiGig RT2 Signal connectors, P1 and P2. Each connector provides up to four 4X gigabit serial ports and this board offers a maximum of eight 4X ports. The VPX specification also defines how many signal and ground connections are available per signal connector.

The 3U VPX board has one XMC mezzanine site that accepts one XMC module.

6U VPX Board

- 6U board outline same as 6U VME
- P0 Utility Connector
 - Power, system reset, reference clock, bus management, addressing, etc.
- MultiGig RT2 for P1 through P6 Signal Connectors
 - Definitions for differential or single-ended signals
 - Up to 24 4X gigabit serial ports
- One or two XMC mezzanine sites

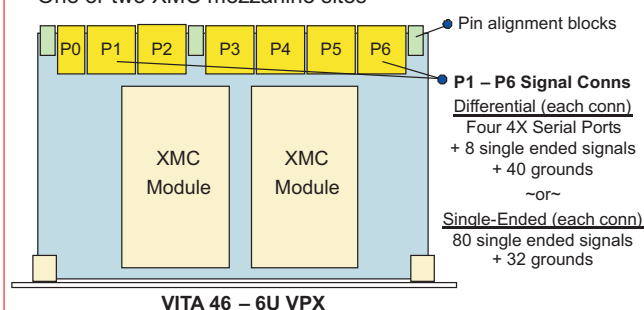


Figure 51

The 6U board outline is the same as the 6U VME board. The board has a P0 Utility connector which provides power, system reset, reference clock, addressing, bus management, and any other required utility functions.

The 6U board has six MultiGig RT2 Signal connectors P1 through P6. Each connector provides up to four 4X gigabit serial ports and this board offers a maximum of 24 4X ports. The VPX specification also defines how many signal and ground connections are available per signal connector.

The 6U VPX board has two XMC mezzanine site and accepts one or two XMC modules.

Switched Serial Fabrics

OpenVPX Initiative

- **Rationale**
 - To embrace VPX as a new system architecture, U.S. DOD mandated industry-wide definition and adoption of standards for VPX technology
 - Provide interoperability across vendors
 - Promote market priced components among competitors
 - Provide long-term availability for life-cycle support
- OpenVPX Industry Organization was formed in January 2009
 - 26 embedded system vendors, manufacturers and contractors
 - Goal: accelerate definition and turn over to VITA for standardization
- **Transition to VITA Standard**
 - Transferred to VSO (VITA Standards Organization) in October 2009
 - Designated as VITA 65
 - Ratified by VITA in February 2010
- **ANSI Standardization**
 - Received in June 2010

Figure 52

The OpenVPX organization was formed in January 2009 to promote industry-wide standards and long-term availability of VPX technology across the industry. The original VPX specification was being used, but because it permitted such a wide range of architectures, VPX systems tended to be unique, vendor-specific implementations.

The mission of OpenVPX was to enhance the original VPX standard by adding a set of well-defined system architectures, nomenclature and conventions to enable interoperability among vendors. Consisting of key vendors in the embedded-system community, all eager to convince government and military customers that VPX was suitable for current and future systems, the group made fast progress and turned over the completed specification to the VSO in October 2009 for standardization under VITA 65. In February 2010, the specification was ratified by VSO and ANSI approval was received in June 2010.



OpenVPX: VITA 65

- Defines sets of system implementations and system architectures
 - Promotes multi-vendor interoperability and life-cycle maintenance
 - Uses existing VITA 46 VPX Baseline and VITA 48 VPX REDI standards
- Defines various sizes of **pipes** used for serial communication
- Defines various **profiles** for structure and hierarchy:
 - slot profiles
 - backplane profiles
 - module profiles
 - development chassis profile
- Defines multiple **planes** for signal types within the specification:
 - Utility
 - Management
 - Control
 - Data
 - Expansion

Figure 53

OpenVPX defined new nomenclature for systems to describe the gigabit serial links in terms of the number of lanes and their function. The term “pipe” is used to define the number of bidirectional differential serial pairs that are grouped together to form a logical data channel.

OpenVPX also categorized the different kinds of traffic carried through the pipes as “planes”. The five planes defined are the utility, management, control, data and expansion planes.

In order to define architectural characteristics of systems, several “profiles” were defined. A slot profile specifies the pipes and planes found on the backplane connectors of each slot. The module profile specifies the pipes, planes, fabrics and protocols implemented on each card. The backplane profile defines how the slots are connected to each other by pipes. And finally, the development chassis profile includes the backplane profile and defines the dimensions, power supply, and cooling method.

Switched Serial Fabrics

OpenVPX Pipes

■ Pipes

- A grouping of differential pairs for an interconnect channel
- Does not specify fabric protocols

Pipe Name	Abbreviation	# Diff Pairs	Also used
Ultra Thin Pipe	UTP	1	X1
Thin Pipe	TP	2	X2
Fat Pipe	FP	4	X4
Double Fat Pipe	DFP	8	X8
Quad Fat Pipe	QFP	16	X16
Octal Fat Pipe	OFP	32	X32



Figure 54

The OpenVPX Pipes are groups of differential pairs that are used to interconnect channels. As shown in the figure above, the defined OpenVPX pipe sizes range from one lane (1X) called an “ultra-thin pipe” or UTP, up to 32 lanes (32X) called an “octal fat pipe” or OFP.

The next size up from UTP is the “thin pipe” or TP which has two lanes or 2X. The popular 4X link is called a “fat pipe” or FP. The next size up from it is the “double fat pipe” or DFP with 8X links.

Next in size is the “quad fat pipe”, QFP or 16X and the fattest one is the “octal fat pipe”, OFP or 32X.

As used here and elsewhere in this handbook, the designation NX is the same as XN, or xN, where N is the number of lanes/pipes; The last designation, xN, is most commonly used with PCI Express 2.0.

OpenVPX Connector Layout

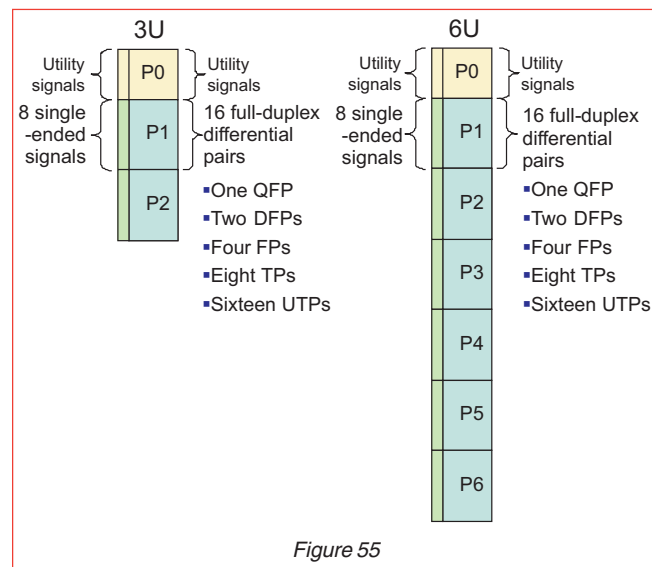


Figure 55

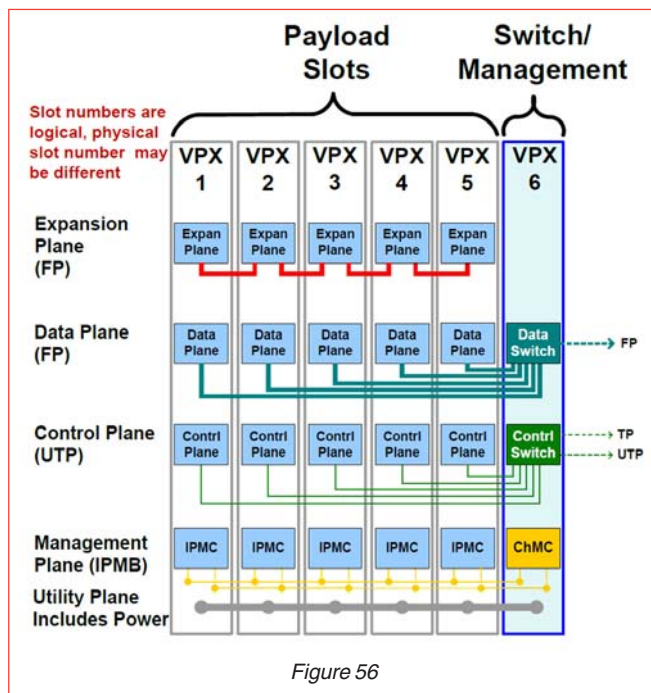
Shown here are the connector layouts for the 3U and 6U cards.

As shown previously, the 3U card has one utility connector for utilities such as power, clock, etc. It also has two signal connectors P1 and P2. Each of these provides connections for eight single-ended signals plus grounds. In addition, each one provides 16 full-duplex differential pairs with the following pipes: sixteen UTPs, eight TPs, four FPs, two DFPs and one QFP.

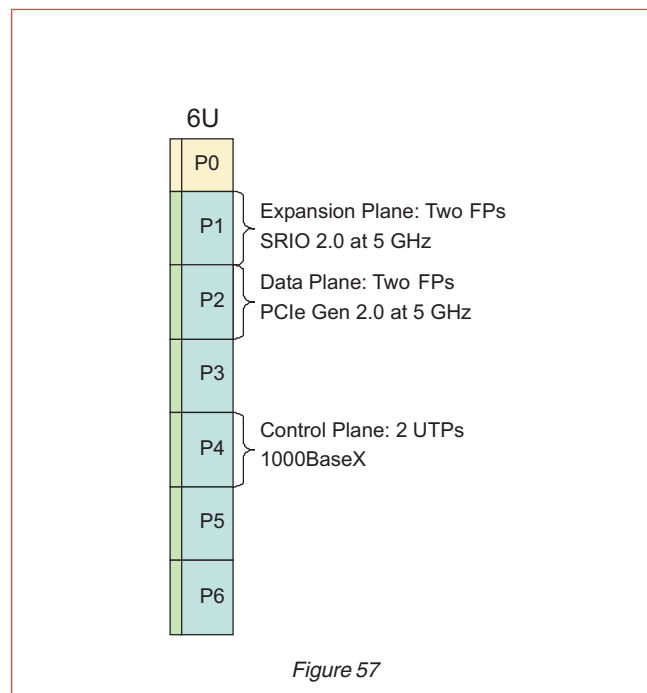
Likewise, the 6U board has the same utility connector and six signal connectors P1 through P6. Each of these provides connections for eight single-ended signals plus grounds. In addition, each one provides 16 full-duplex differential pairs with the following pipes: sixteen UTPs, eight TPs, four FPs, two DFPs and one QFP.

Switched Serial Fabrics

Typical OpenVPX Backplane Profile



Typical OpenVPX Module Profile



The OpenVPX specification established quite a large number of backplane profiles. The backplane profile is a physical definition of a backplane implementation. Included in this definition are:

- Slot sizes such as 3U or 6U
- Slot spacing such as 1.00, 0.85, or 0.80 inches
- Quantity of slots and type of slots
- Topologies used to interconnect the slots, such as:
 - ◆ Mesh
 - ◆ Central switch
 - ◆ Distributed
 - ◆ Root-leaf

Shown here is a typical 6-slot backplane with five payload cards and one switch/management card. Backplanes such as this one are primarily intended for development environments. However, some systems could be deployed in the field with these backplanes.

In addition to the backplane profiles, OpenVPX specifies module profiles. The module profile provides a physical mapping of ports into the module's backplane connectors. The module profile includes the assignment of specific protocols used for each port. It also provides first-order compatibility checks between modules and slots.

The typical module profile above shows the assignments for P1, P2, and P4. P0 is used for the utility functions. The assignments for the balance of connectors may be user-specified to suit the application.

Switched Serial Fabrics

VPX Specification Status

■ VITA 46.0 – VPX Baseline Specification	Approved
• VITA 46.1 VMEbus Signal Mapping	Approved
• VITA 46.3 Serial RapidIO on VPX	Draft
• VITA 46.4 PCI Express on VPX	Draft
• VITA 46.6 Gbit Ethernet Control Plane on VPX	Draft
• VITA 46.7 Ethernet on VPX Fabric Connector	Draft
• VITA 46.9 PMC/XMC Rear I/O to 3U/6U Pin Mapping	Draft
• VITA 46.10 Rear Transition Module for VPX	Draft
• VITA 46.20 VPX Switch Slot Definition	Draft
• VITA 46.21 Distributed Switching Topologies on VPX	Draft
■ VITA 48.0 – REDI	Draft
• VITA 48.1 – REDI Air Cooling	Draft
• VITA 48.2 – REDI Conduction Cooling	Draft
• VITA 48.3 – REDI Liquid Cooling	Draft
• VITA 48.5 – Air Flow Through Cooling	Draft
■ VITA 65 – OpenVPX	
• VITA 65.0 Base Specification 1.05	Approved Feb 2010
• ANSI Adoption	Approved Jun 2010
■ VITA 66 – Fibre Optic Interconnect	
• VITA 66.0 Base Specification 0.4	Draft
• VITA 66.1 MT Optical Interconnect Spec 0.51	Draft
■ VITA 67 – Analog/RF Coaxial Interconnect	
• VITA 67.0 Base Specification 0.46	Draft

Figure 58

As of this writing, the VPX Baseline Specification has been approved by both VITA and ANSI and has been released as VITA 46.0

Also approved by VITA and ANSI and released is VITA 46.1, the VMEbus Signal Mapping. The balance of the VITA 46 subspecifications are in draft form.

Likewise, the VITA 48 REDI and all its subspecifications are in draft form.

Finally, the OpenVPX VITA 65.0 Base Specification 1.05 was approved by VITA in February 2010. As of this writing (June 2010), this Specification has been advanced to 1.15 and was just approved by ANSI on June 15.

Two more VITA standards are in draft form: VITA 66 Fibre Optic Interconnect and VITA 67 Analog/RF Coaxial Interconnect. The latter has been initiated by DRS and Pentek has been actively involved in the development of this specification.

For more information regarding VITA/ANSI standards, contact:

VMEbus International Trade Association

<http://www.vita.com>



Products

MPC8641D PowerPC Processor with Virtex-4 FPGA - VME/VXS

Model 4207

- MPC8641 single or dual core PowerPC processor to 1.5 GHz
- Xilinx Virtex-4 FX Series FPGA
- Hosts two PMC or XMC modules
- On-board dual gigabit Ethernet interfaces
- Optional on-board 4-Gbit dual optical Fibre Channel controller
- Optional dual optical gigabit serial Fibre Channel interface
- Up to 2 GB DDR2 SDRAM
- Two 64-bit PCI-X buses
- VME64x master/slave interface
- Optional VXS interface
- **Ruggedized and conduction-cooled versions**

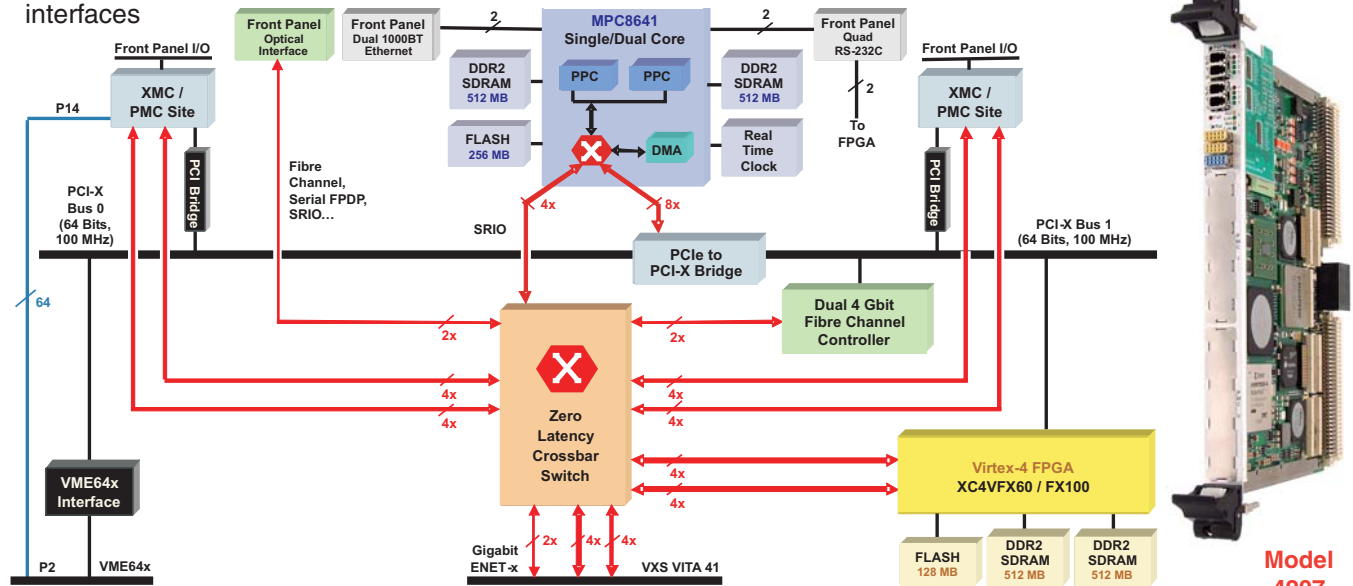


Figure 59

The Pentek Model 4207 PowerPC® VME/VXS I/O processor board targets embedded applications that require high-performance I/O and processing. With two PMC/XMC module sites, the 4207 offers powerful one-slot solutions with nearly unlimited high-speed connectivity.

Utilizing a unique crossbar switch architecture, the 4207 allows you to make the connections you want between board resources and high-speed interfaces. You don't need hardwiring, or FPGA space to define your I/O data flow and resource assignment.

The Freescale® MPC8641 utilizes the AltiVec® engine to perform parallel processing of multiple data elements (SIMD) with 128-bit operations. The AltiVec processor executes both fixed- and floating-point instructions. It is available with either single or dual e600 PowerPC core with maximum clock frequency of 1.5 GHz.

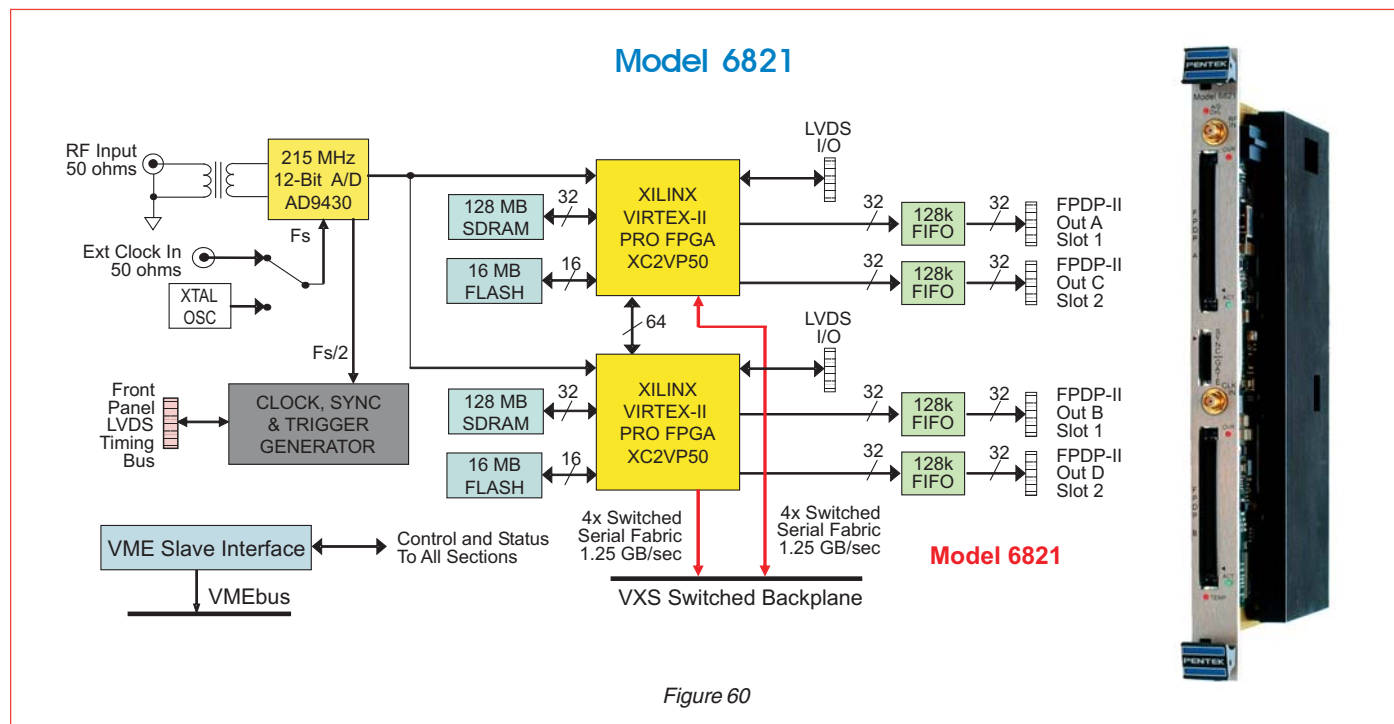
The 4207 may be optionally equipped with a Xilinx Virtex-4 FX FPGA, either the XC4VFX60 or the XC4VFX100. Two 4X RocketIO ports provide high-speed serial data paths to and from the FPGA.

Unused FPGA resources are available for the user to implement custom signal-processing configurations and algorithms using Pentek's GateFlow FPGA Design Kit and the high-performance IP Core Library.

The Model 4207 is supported with world-class software for initialization, control and optimization. In addition to GateFlow, this includes real-time OS support for VxWorks and Linux, ReadyFlow board support package and VSIPL scientific and engineering functions.

Products

215 MHz, 12-bit A/D with Virtex-II FPGAs - VME/VXS



The Model 6821 is a 6U single slot board with the AD9430 12-bit 215 MHz A/D converter.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

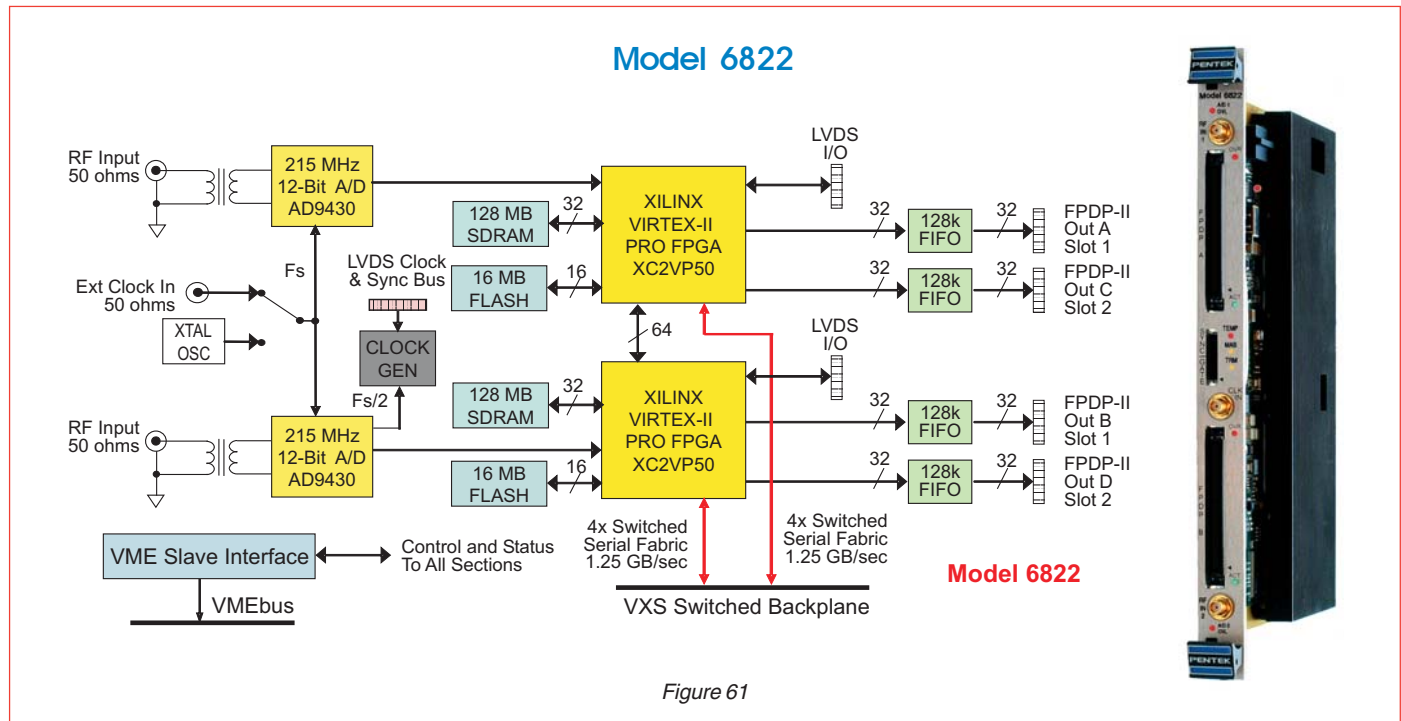
Optional 4X switched serial fabric ports, compliant with the VITA 41 VXS backplane fabric standard, deliver data to VXS devices using two full-duplex 1.25 GB/sec data ports.

Since the switched fabric interface is implemented using the Rocket I/O gigabit serial transceivers in the FPGAs, the Model 6821 can support any of the switched fabric protocols including Serial RapidIO, PCI Express or the lightweight point-to-point link layer protocol, Aurora.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications.

Products

Dual 215 MHz, 12-bit A/D with Virtex-II FPGAs - VME/VXS



The Model 6821 is a 6U single slot board with two AD9430 12-bit 215 MHz A/D converters.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

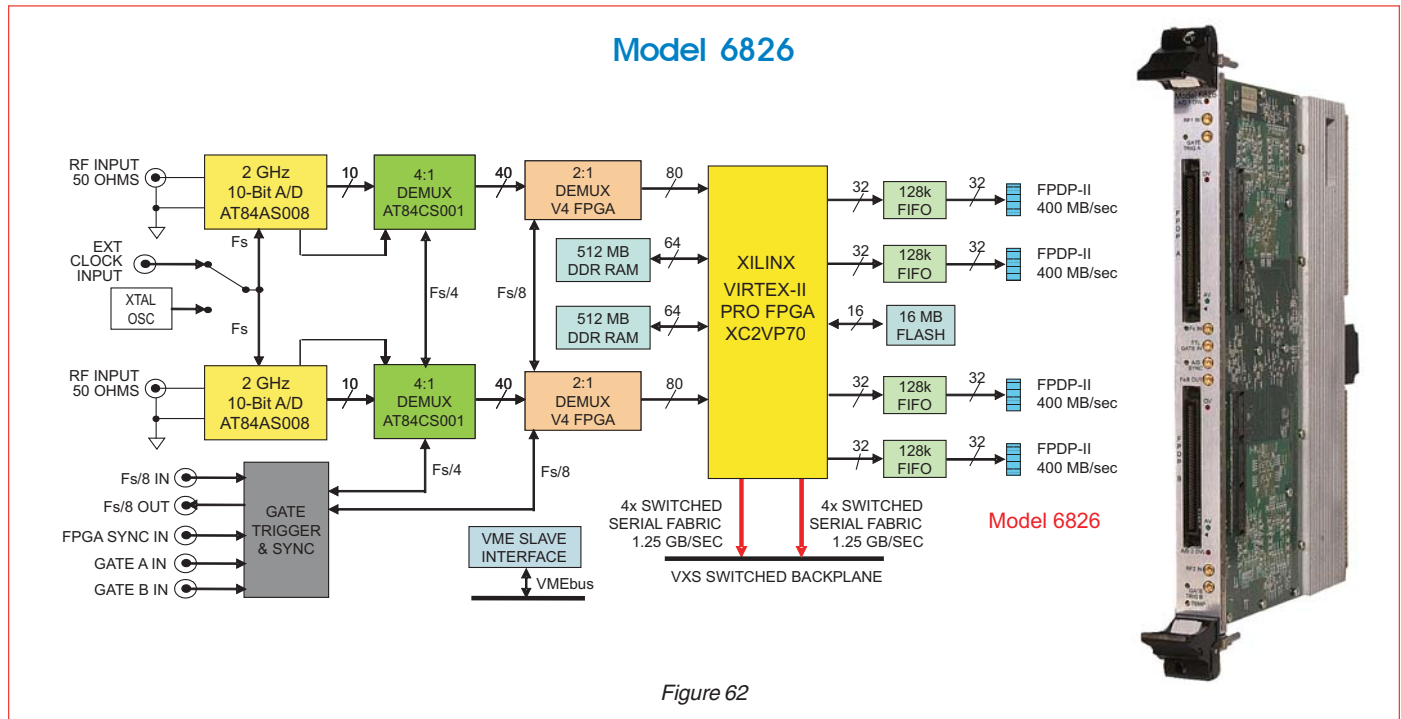
Optional 4X switched serial fabric ports, compliant with the VITA 41 VXS backplane fabric standard, deliver data to VXS devices using two full-duplex 1.25 GB/sec data ports.

Since the switched fabric interface is implemented using the Rocket I/O gigabit serial transceivers in the FPGAs, the Model 6822 can support any of the switched fabric protocols including Serial RapidIO, PCI Express, or the lightweight point-to-point link layer protocol Aurora.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications.

Products

Dual 2 GHz A/D with Xilinx Virtex-II Pro FPGA - VME/VXS



The Model 6826 is a 6U single slot VME board with two Atmel AT84AS008 10-bit 2 GHz A/D converters.

Capable of digitizing input signals at sampling rates up to 2 GHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz.

Data from each of the two A/D converters flows into an innovative dual-stage demultiplexer that packs groups of eight data samples into 80-bit words for delivery to the Xilinx Virtex-II Pro XC2VP70 FPGA at one eighth the sampling frequency. This advanced circuit features the Atmel AT84CS001 demultiplexer which represents a significant improvement over previous technology.

Two 512 MB or 1 GB SDRAMs, support large memory applications such as swinging buffers, digital

filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGA to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGA over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

The 400 MB/sec FPDP ports run out of speed at an A/D sample rate of 1.6 GHz for one channel.

With VXS, however, the two 1.25 GB/sec ports can maintain continuous streaming data at up to 2.5 GB/sec, nicely handling the full 2 GHz A/D speed for one channel.

This Model is also available in a single-channel version and in commercial as well as conduction-cooled versions.

Products

Multiband Transceivers

Model 7141 PMC/XMC • Model 7241 6U cPCI • Model 7341 3U cPCI • Model 7641 PCI
• Model 7741 Full-length PCIe • Model 7841 Half-length PCIe • Model 5341 3U VPX

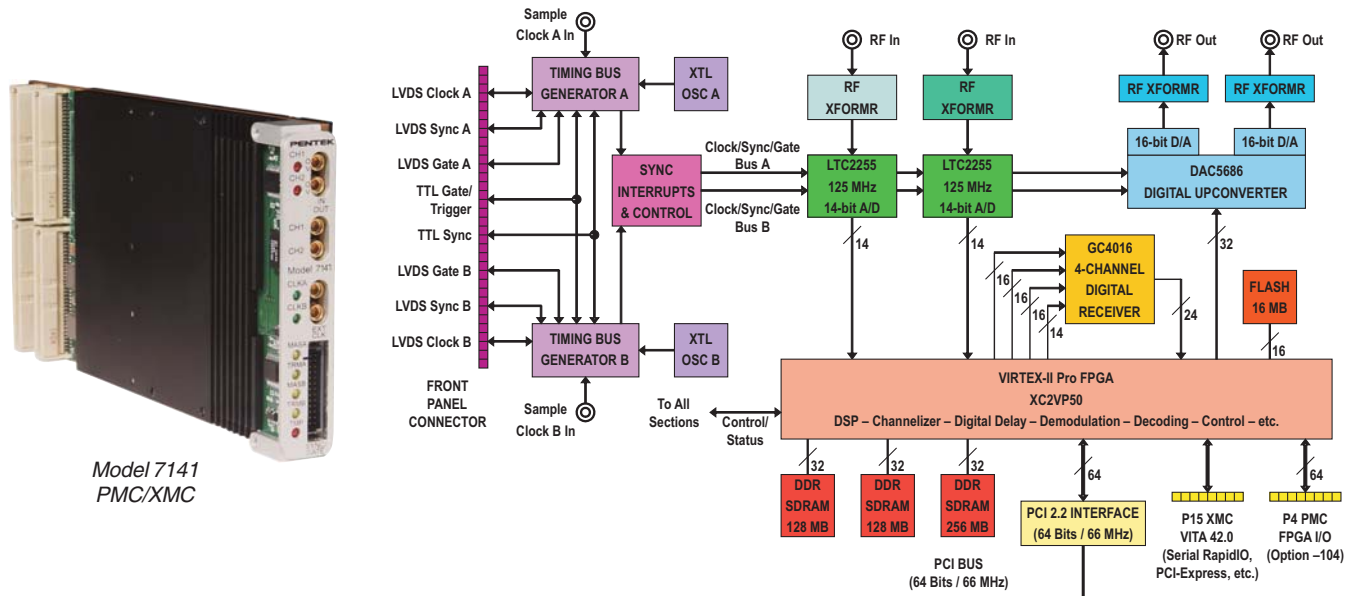


Figure 63

The Model 7141 is a complete transceiver PMC/XMC module. It includes two 125 MHz 14-bit A/D converters and two 500 MHz 16-bit D/A converters to support two wideband receive and transmit communication channels.

The Xilinx Virtex-II Pro FPGA features 6 million gates of logic density and 232 hardware multipliers for implementing DSP functions.

It also features 512 MB of SDRAM for implementing transient capture of up to 1.28 seconds of A/D data for radar applications or digital delay memory for signal intelligence tracking applications at 100 MHz.

A 16 MB flash memory supports the boot code for the two on-board IBM 405 PowerPC microcontroller cores within the FPGA.

A 9-channel DMA controller and 64 bit / 66 MHz PCI interface assures fast efficient transfers among module data sources.

A GC4016 four-channel narrowband digital down-converter can be sourced from the A/D converters, from the delay memory, or from the PCI bus.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the new XMC connector with two 1.25 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phase of the communication channels must be preserved.

Versions of the 7141 are also available as a PCIe full-length board (Models 7741 and 7741D dual density), PCIe half-length board (Model 7841), 3U VPX board (Model 5341), PCI board (Model 7641), 6U cPCI (Models 7241 and 7241D dual density), and 3U cPCI (Model 7341).

Model 7141-703 is a conduction-cooled version.

Products

Multichannel SDR Transceivers

**Model 7142 PMC/XMC • Model 7242 6U cPCI • Model 7342 3U cPCI • Model 7642 PCI
Model 7742 Full-length PCIe • Model 7842 Half-length PCIe • Model 5342 3U VPX**

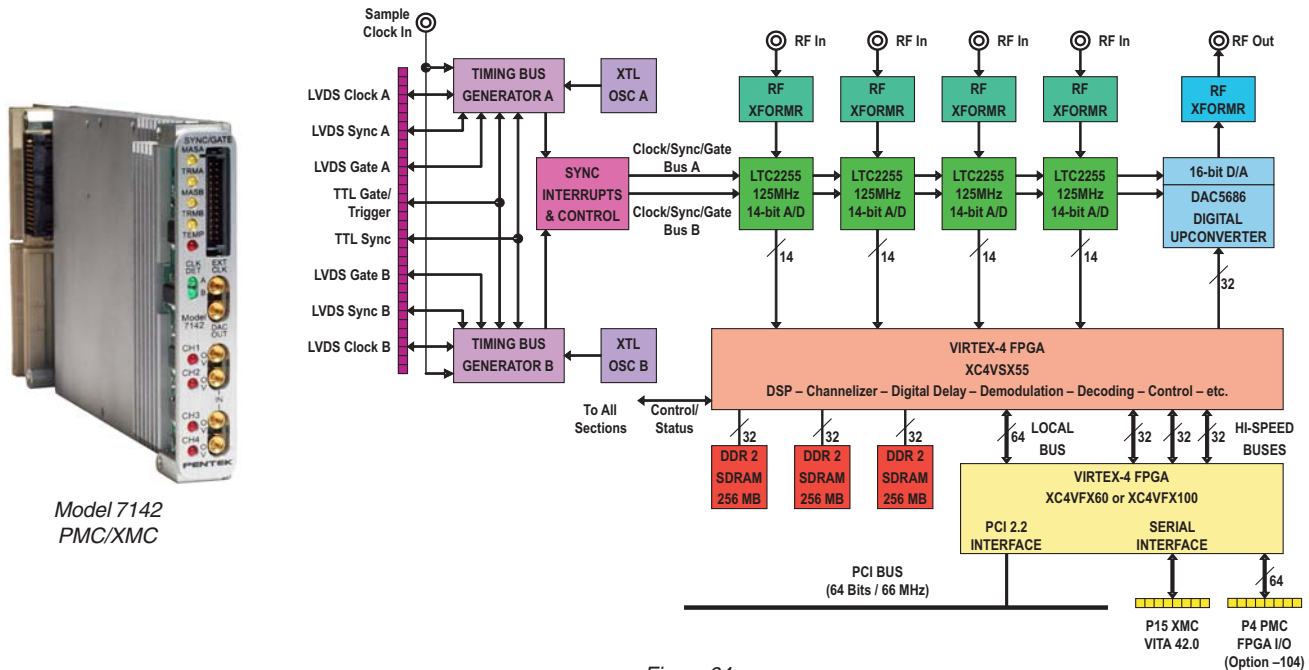


Figure 64

The Model 7142 is a Multichannel PMC/XMC module. It includes four 125 MHz 14-bit A/D converters and one upconverter with a 500 MHz 16-bit D/A converter to support wideband receive and transmit communication channels.

Two Xilinx Virtex-4 FPGAs are included: an XC4VSX55 or LX100 and an XC4VFX60 or FX100. The first FPGA is used for control and signal processing functions, while the second one is used for implementing board interface functions including the XMC interface.

It also features 768 MB of SDRAM for implementing up to 2.0 sec of transient capture or digital delay memory for signal intelligence tracking applications at 125 MHz.

A 16 MB flash memory supports the boot code for the two on-board IBM 405 PowerPC microcontroller cores within the FPGA.

A 9-channel DMA controller and 64 bit / 66 MHz PCI interface assures efficient transfers to and from the module.

A high-performance 160 MHz IP core wideband digital downconverter may be factory-installed in the first FPGA.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the second FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7142 are also available as a PCIe full-length board (Models 7742 and 7742D dual density), PCIe half-length board (Model 7842), 3U VPX (Model 5342), PCI board (Model 7642), 6U cPCI (Models 7242 and 7242D dual density), and 3U cPCI (Model 7342).

Products

Quad 200 MHz 16-bit A/D with Virtex-5 FPGAs

Model 7150 PMC/XMC • Model 7250 6U cPCI • Model 7350 3U cPCI • Model 7650 PCI
 Model 7750 Full-length PCIe • Model 7850 Half-length PCIe • Model 5350 3U VPX

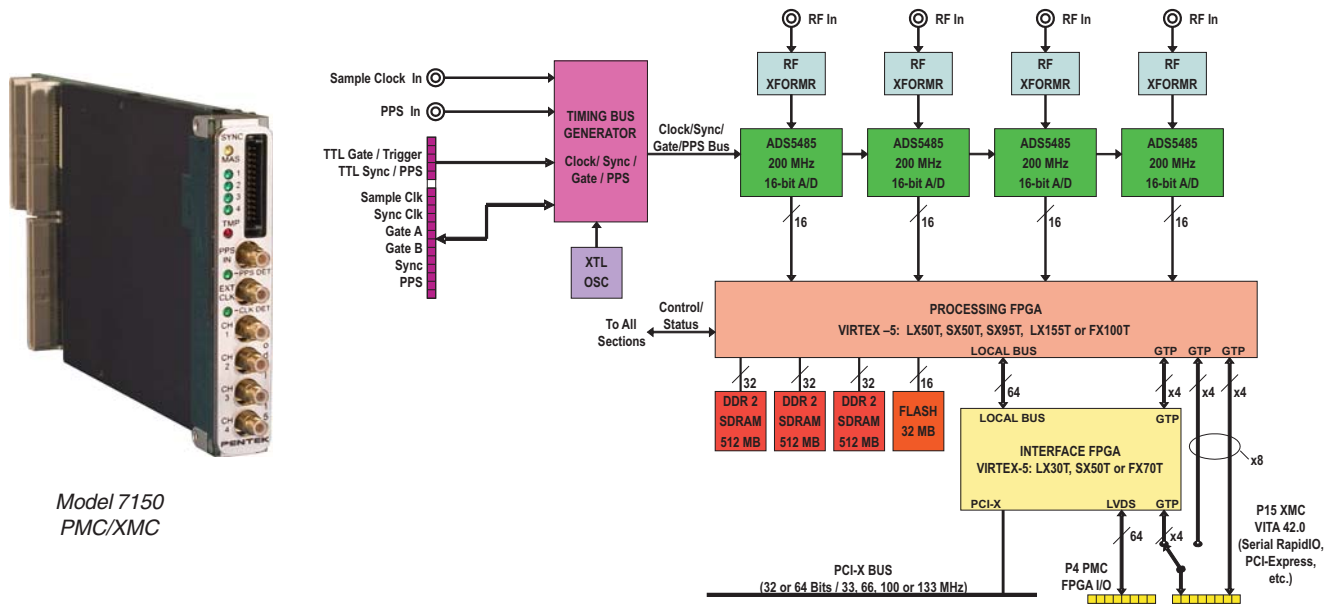


Figure 65

Model 7150 is a quad, high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds supported by an array of data processing and transport resources ideally matched to the requirements of high-performance systems. Model 7150 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched fabric interfaces.

The Model 7150 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Three independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient

capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 9-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7150 are also available as a PCIe full-length board (Models 7750 and 7750D dual density), PCIe half-length board (Model 7850), PCI board (Model 7650), 6U cPCI (Models 7250 and 7250D dual density), 3U cPCI (Model 7350), and 3U VPX (Model 5350).

Products

Quad 200 MHz 16-bit A/D with 256-Channel DDC Installed Core

Model 7151 PMC • Model 7251 6U cPCI • Model 7351 3U cPCI • Model 7651 PCI
 Model 7751 Full-length PCIe • Model 7851 Half-length PCIe • Model 5351 3U VPX

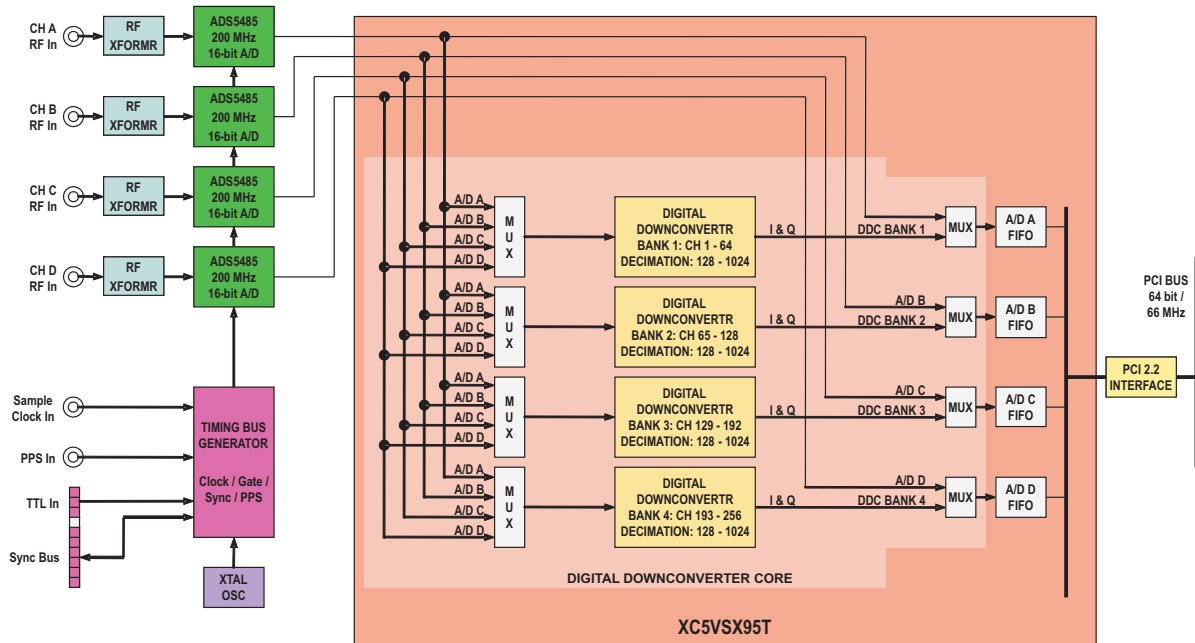


Figure 66

The Model 7151 PMC module is a 4-channel high-speed digitizer with a factory-installed 256-channel DDC core. The front end of the module accepts four RF inputs and transformer-couples them into four 16-bit A/D converters running at 200 MHz. The digitized output signals pass to a Virtex-5 FPGA for routing, formatting and DDC signal processing.

The Model 7151 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 256 DDCs has an independent 32-bit tuning frequency setting.

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting

as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples. Any number of channels can be enabled within each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Versions of the 7151 are also available as a PCIe full-length board (Models 7751 and 7751D dual density), PCIe half-length board (Model 7851), PCI board (Model 7651), 6U cPCI (Models 7251 and 7251D dual density), 3U cPCI (Model 7351), and 3U VPX (Model 5351).

Products

4-Channel Beamformer Installed Core with four 200 MHz, 16-bit A/Ds

Model 7153 PMC/XMC • Model 7253 6U cPCI • Model 7353 3U cPCI • Model 7653 PCI
 Model 7753 Full-length PCIe • Model 7853 Half-length PCIe • Model 5353 3U VPX

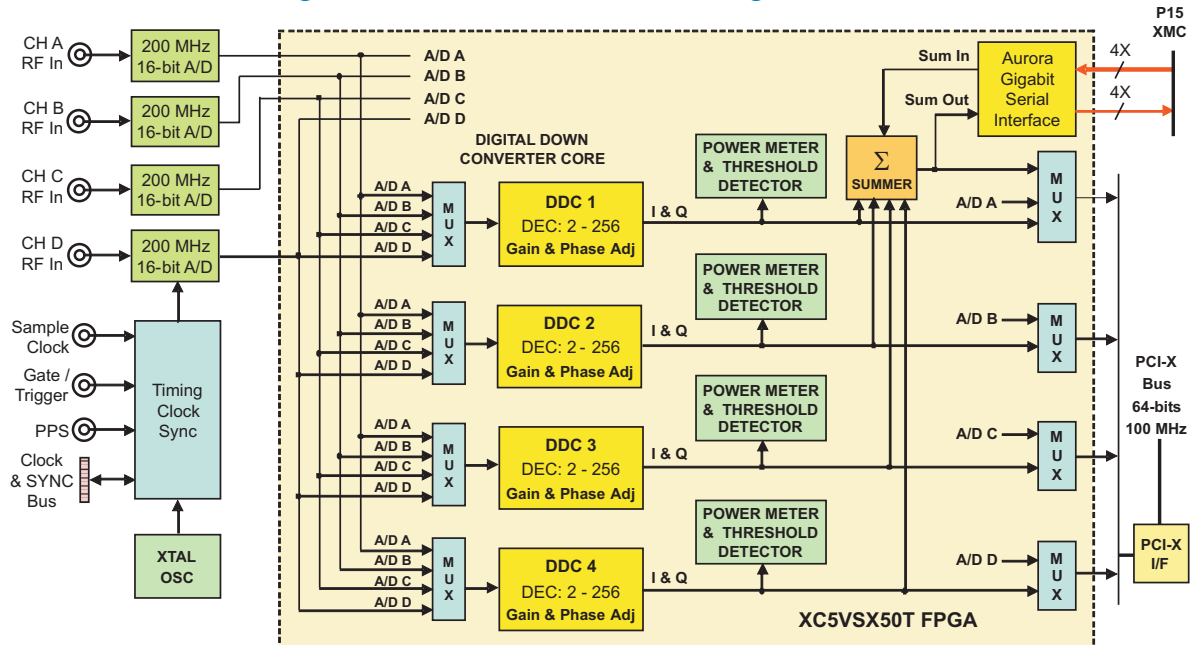


Figure 67

Model 7153 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel DDC (digital downconverter) installed core and a complete set of beamforming functions. With built-in multiboard synchronization and an Aurora gigabit serial interface, it provides everything needed for implementing multichannel beamforming systems.

The Model 7153 employs an advanced FPGA-based DDC engine consisting of four identical multiband banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 4 DDCs has an independent 32-bit tuning frequency setting.

All four DDCs have a decimation setting that can range from 2 to 256, programmable independently in steps of 1. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of

$0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output band-width is better than 100 dB.

In addition to the DDCs, the 7153 features a complete beamforming subsystem. Each channel contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 ksamples. The power meters present average power measurements for each channel in easy-to-read registers. Each channel also includes a threshold detector that sends an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

Versions of the 7153 are also available as a PCIe full-length board (Models 7753 and 7753D dual density), PCIe half-length board (Model 7853), PCI board (Model 7653), 6U cPCI (Models 7253 and 7253D dual density), 3U cPCI (Model 7353), and 3U VPX (Model 5353).

Products

Dual 400 MHz 14-bit A/D and 800 MHz D/A with Virtex-5 FPGAs

Model 7156 PMC/XMC • Model 7256 6U cPCI • Model 7356 3U cPCI • Model 7656 PCI
 Model 7756 Full-length PCIe • Model 7856 Half-length PCIe • Model 5356 3U VPX

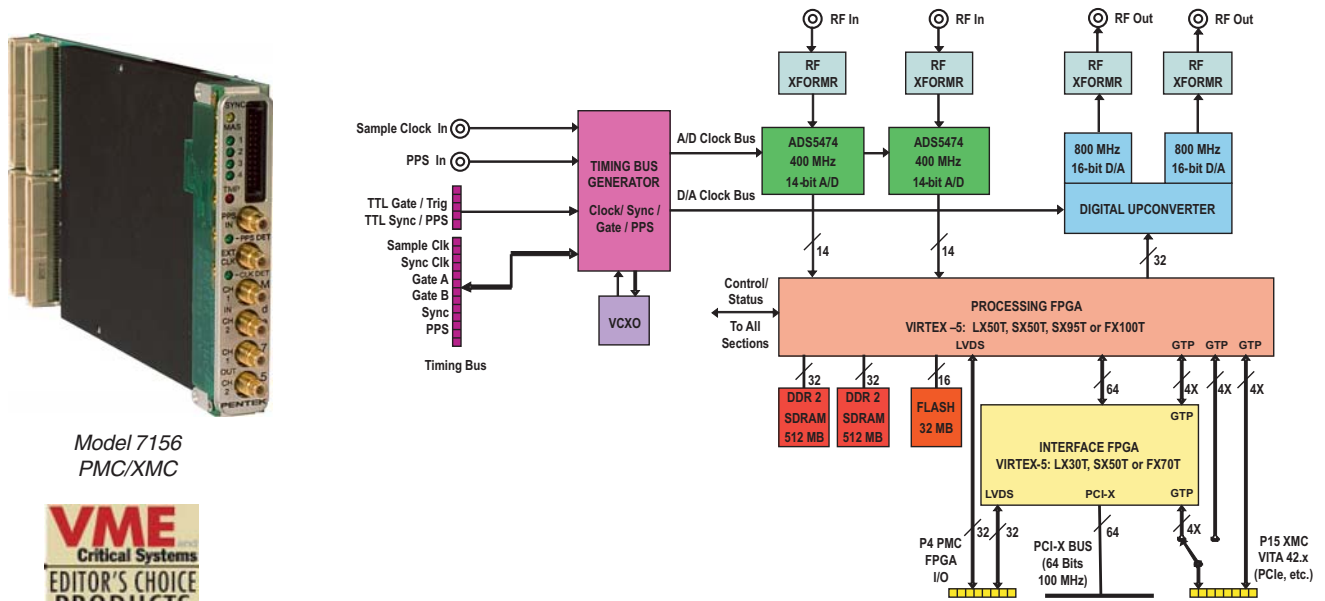


Figure 68

Model 7156 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 400 MHz 14-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7156 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7156 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 5-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7156 are also available as a PCIe full-length board (Models 7756 and 7756D dual density), PCIe half-length board (Model 7856), PCI board (Model 7656), 6U cPCI (Models 7256 and 7256D dual density), 3U cPCI (Model 7356), and 3U VPX (Model 5356). All these products have similar features.

Products

Dual 500 MHz 12-bit A/D and 800 MHz D/A with Virtex-5 FPGAs

**Model 7158 PMC/XMC • Model 7258 6U cPCI • Model 7358 3U cPCI • Model 7658 PCI
Model 7758 Full-length PCIe • Model 7858 Half-length PCIe • Model 5358 3U VPX**

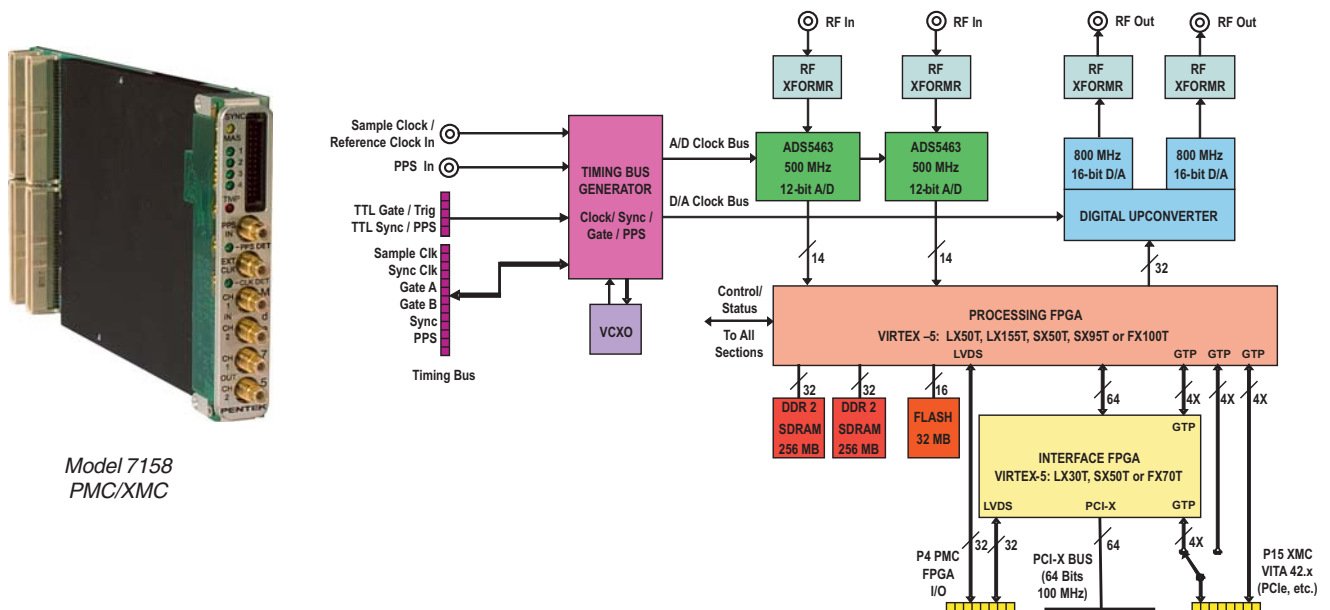


Figure 69

Model 7158 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 500 MHz 12-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7158 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7158 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 256 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 5-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

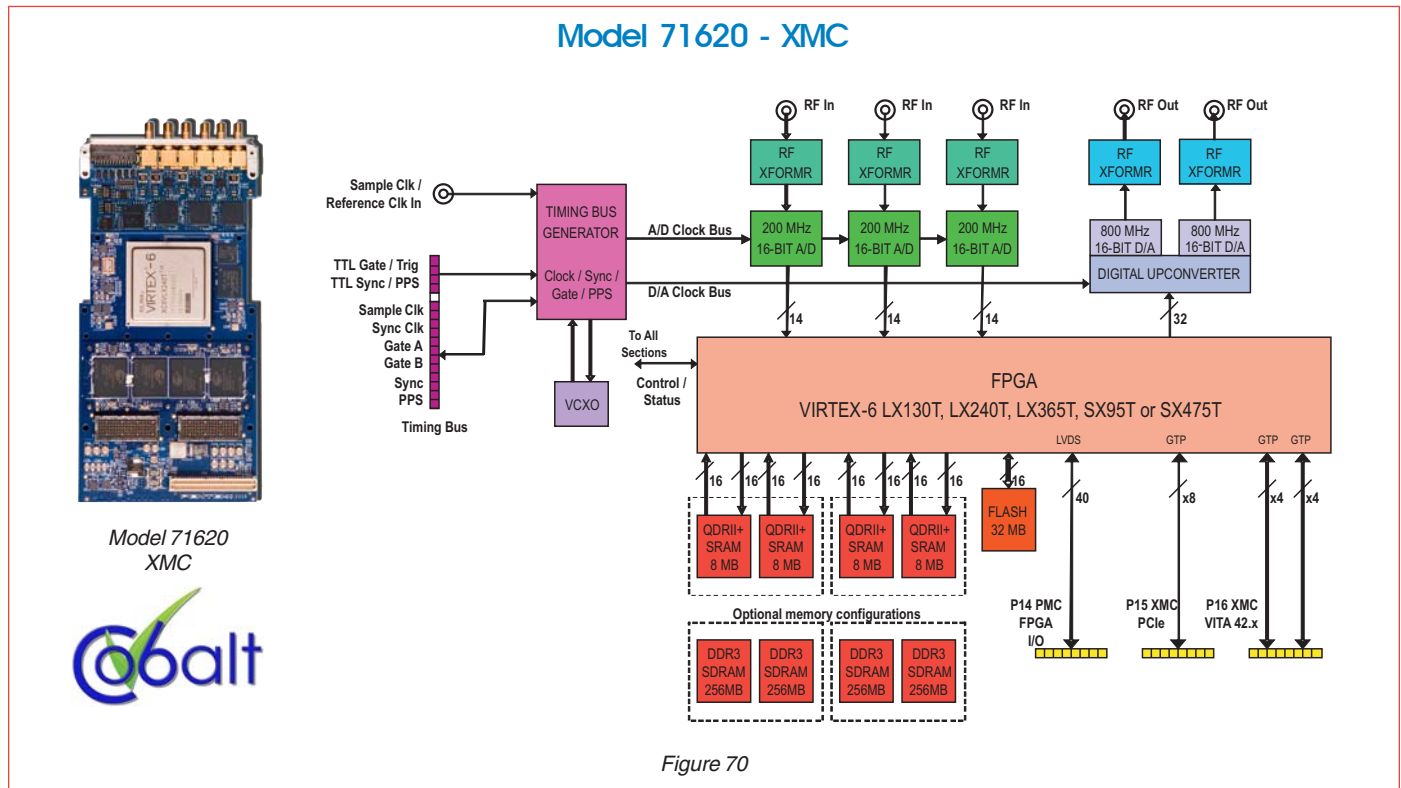
Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7158 are also available as a PCIe full-length board (Models 7758 and 7758D dual density), PCIe half-length board (Model 7858), PCI board (Model 7658), 6U cPCI (Models 7258 and 7258D dual density), 3U cPCI (Model 7358), and 3U VPX (Model 5358). All these products have similar features.

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA



Model 71620 is the first member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications and radar system. It includes three 200 MHz, 16-bit A/Ds, one DUC, two 800 MHz 16-bit D/As, and four banks of memory. The Model 71620 is compatible with the VITA 42.0 XMC format and supports PCI Express Gen. 2.

The Model 71620 Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The FPGA serves as a control and status engine with data and programming interfaces to each of the on-board

resources including the data converters, DDR3 SDRAM or QDRII+ SRAM memory, PCIe interface, programmable LVDS I/O and clock, gate, and synchronization circuits. The FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-6 LX130T, LX240T, LX365T, SX315T, or SX475T.

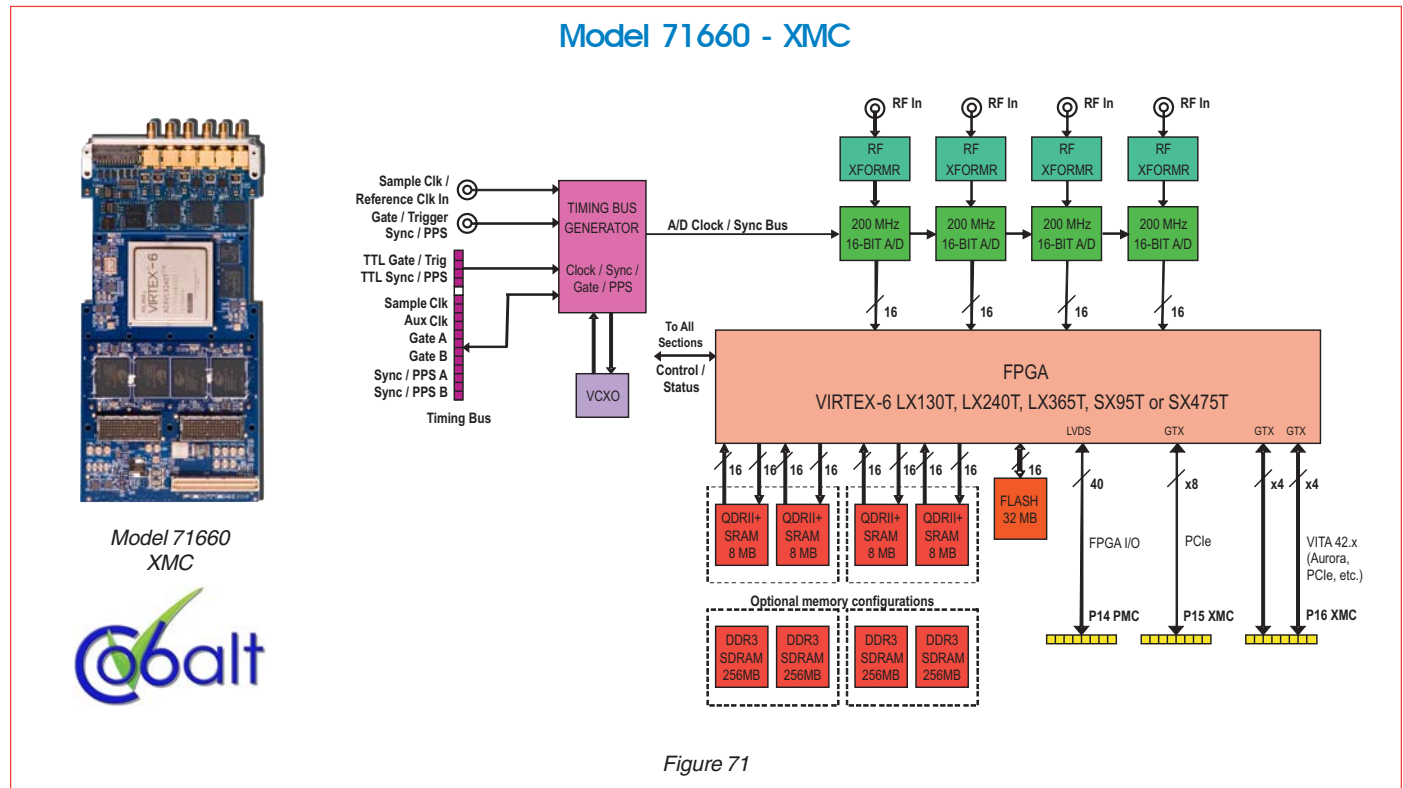
Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

The 71620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

The Model 71620 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Products

4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA



Model 71660 is a member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications and radar system. It includes four 200 MHz 16-bit A/Ds, and four banks of memory. The Model 71660 is compatible with the VITA 42.0 XMC format and supports PCI Express Gen. 2.

The Model 71660 Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The FPGA serves as a control and status engine with data and programming interfaces to each of the on-board

resources including the data converters, DDR3 SDRAM or QDRII+ SRAM memory, PCIe interface, programmable LVDS I/O and clock, gate, and synchronization circuits. The FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-6 LX130T, LX240T, LX365T, SX315T, or SX475T.

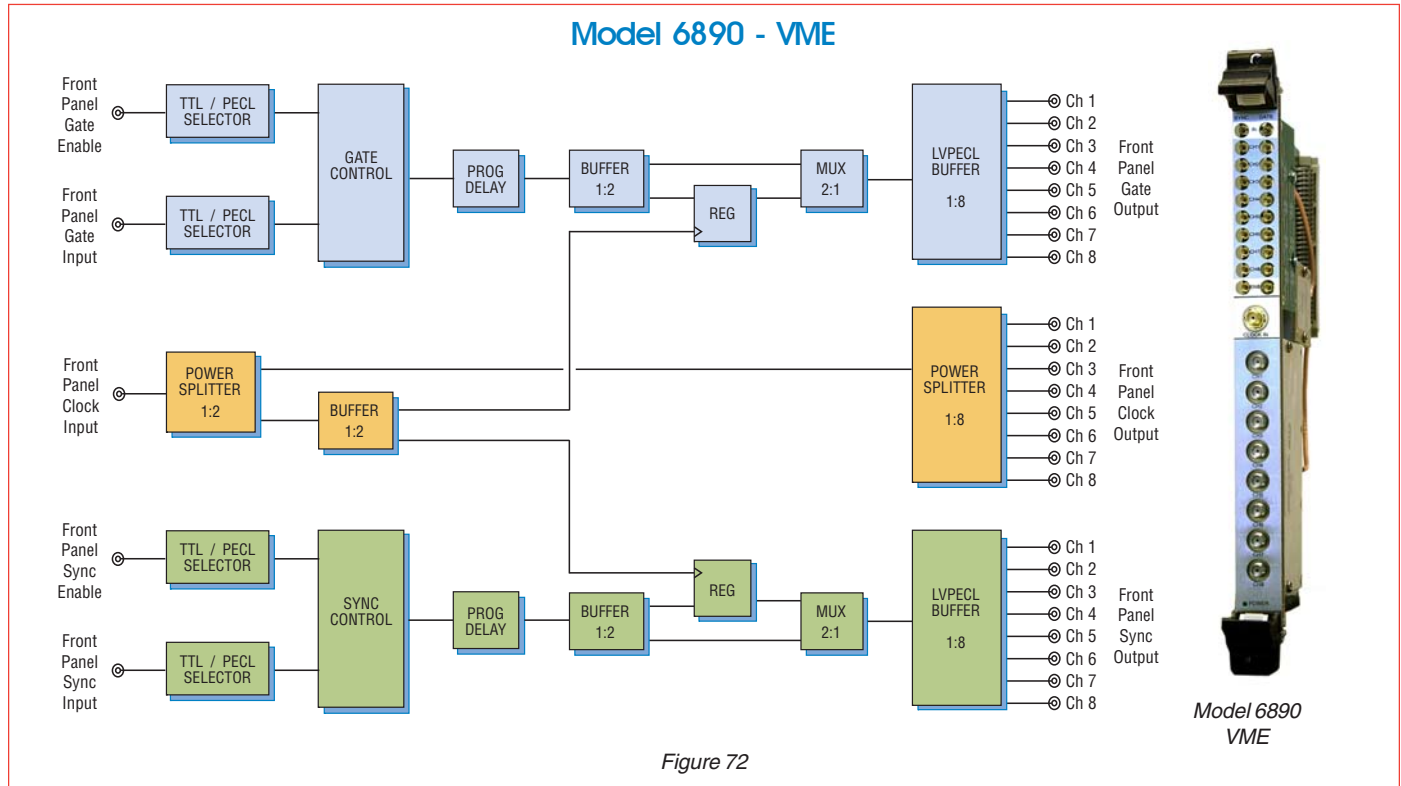
Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

The 71660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

The Model 71660 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Products

2.2 GHz Clock, Sync and Gate Distribution Board



Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors. The second output of the 1:2 power

splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.

The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable inputs allow the user to enable or disable these circuits using an external signal.

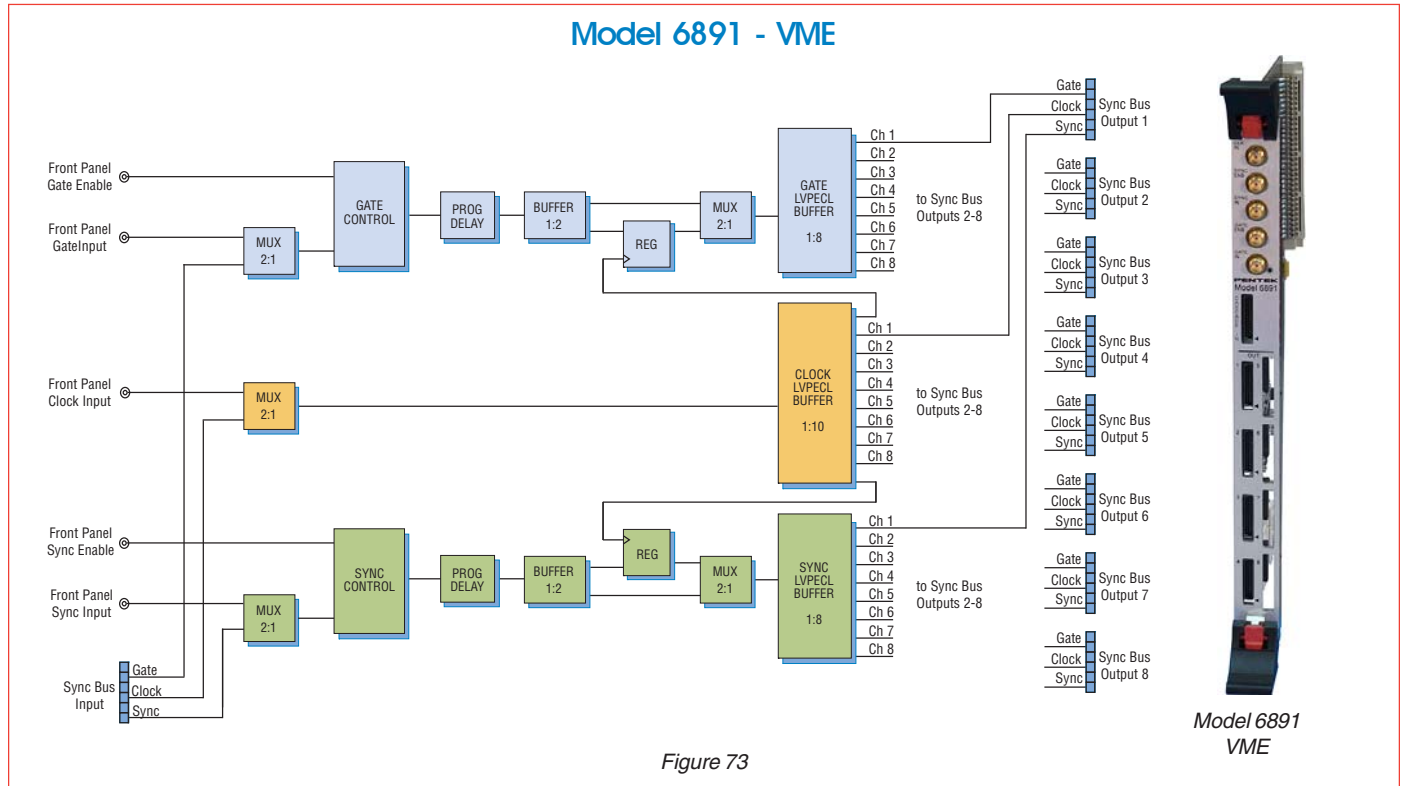
A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/trigger and sync signals to be registered with the input clock signal before output, if desired.

Sets of input and output cables for two to eight boards are available from Pentek.

Products

System Synchronizer and Distribution Board



Model 6891 System Synchronizer and Distribution Board synchronizes multiple Pentek I/O modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight modules can be synchronized using the 6891, each receiving a common clock up to 500 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 6891's can be linked together to provide synchronization for up to 64 I/O modules producing systems with up to 256 channels.

Model 6891 accepts three TTL input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Two additional inputs are provided for separate gate and sync enable signals.

Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. Alternately, a Sync Bus connector accepts LVPECL inputs from any compatible Pentek products to drive the clock, sync and gate/trigger signals.

The 6891 provides eight front panel Sync Bus output connectors, compatible with a wide range of Pentek I/O modules. The Sync Bus is distributed through ribbon cables, simplifying system design. The 6891 accepts clock input at +10 dBm to +14 dBm with a frequency range from 1 kHz to 800 MHz. This clock is used to register all sync and gate/trigger signals as well as providing a sample clock to all connected I/O modules.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer for output through the Sync Bus connectors.

Products

Multifrequency Clock Synthesizer

**Model 7190 PMC • Model 7290 6U cPCI • Model 7390 3U cPCI • Model 7690 PCI
Model 7790 Full-length PCIe • Model 7890 Half-length PCIe • Model 5390 3U VPX**

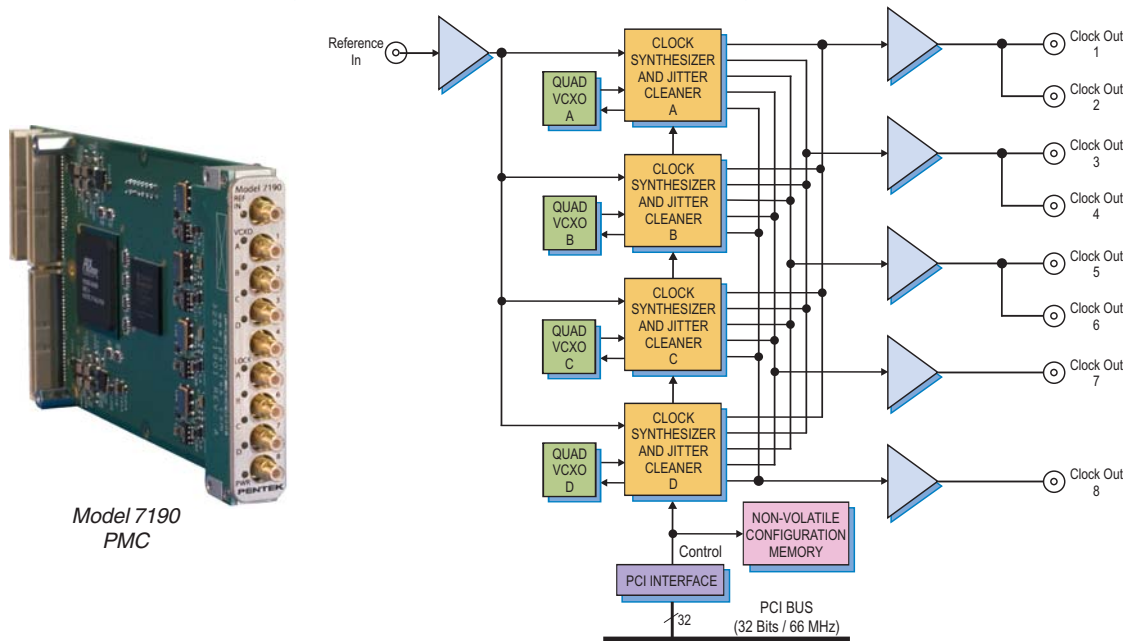


Figure 74

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from an input reference signal using phase-locked oscillators.

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each device includes phase-locking circuitry that locks the frequency of its associated quad VCXO (Voltage Controlled Crystal Oscillator) to the input reference clock. This reference is a 5 or 10 MHz signal supplied to a front panel SMC connector. Each quad VCXO is programmed to generate one of four base frequencies.

Each CDC7005 generates five output signals. Each signal is independently programmable as a submultiple of the associated VCXO base frequency using divisors of 1, 2, 4, 8 or 16.

The five clock output signals from each of the four CDC7005s are joined into five clock buses. Each output can be independently enabled to drive each bus, thereby allowing any combination of output signals from the four CDC7005s.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock buses, as shown in the block diagram. This supports a single identical clock to all eight outputs or five different clocks to various outputs; numerous other combinations are possible.

The 7190 is equipped with a non-volatile memory. Once configured, the settings return to the saved configuration upon power up.

Versions of the 7190 are also available as a PCIe full-length board (Models 7790 and 7790D dual density), PCIe half-length board (Model 7890), 3U VPX board (Model 5390), PCI board (Model 7690), 6U cPCI (Models 7290 and 7290D dual density), or 3U cPCI (Model 7390).

Products

Clock and Sync Generator for I/O Modules

Model 9190 - Rack-mount

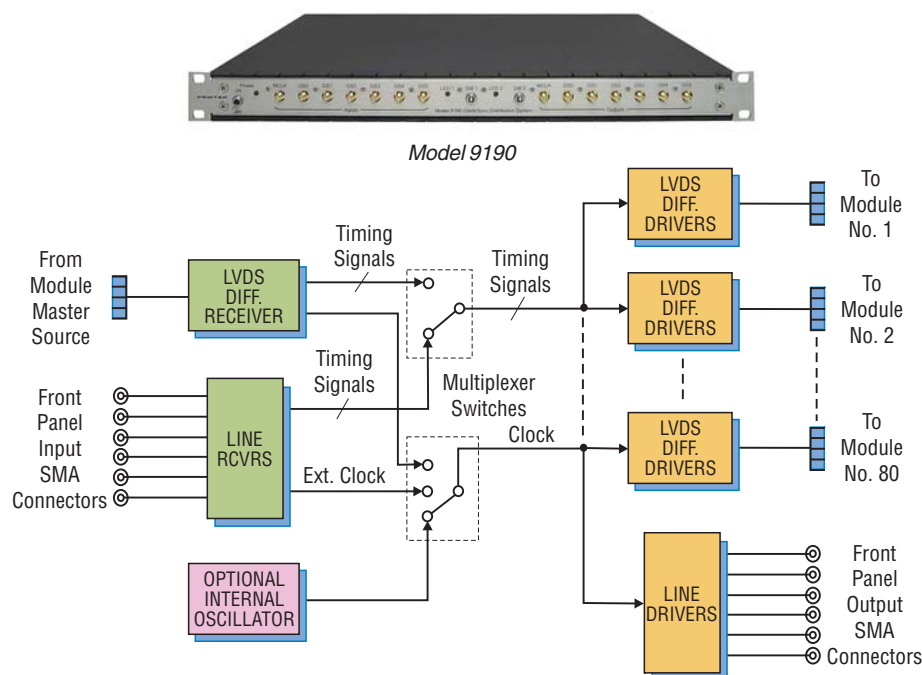


Figure 75

Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.

Clock and timing signals can come from six front panel SMA user inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the Model 9190.

Buffered versions of the clock and five timing signals are available as outputs on the 9190's front panel SMA connectors.

Model 9190 is housed in a line-powered, 1.75 in. high metal chassis suitable for mounting in a standard 19 in. equipment rack, either above or below the cage holding the I/O modules.

Separate cable assemblies extend from openings in the front panel of the 9190 to the front panel clock and sync connectors of each I/O module. Mounted between two standard rack-mount card cages, Model 9190 can drive a maximum of 80 clock and sync cables, 40 to the card cage above and 40 to the card cage below. Fewer cables may be installed for smaller systems.

Products

Rack-mount Real-Time Recording and Playback Transceiver Instrument

Model RTS 2701

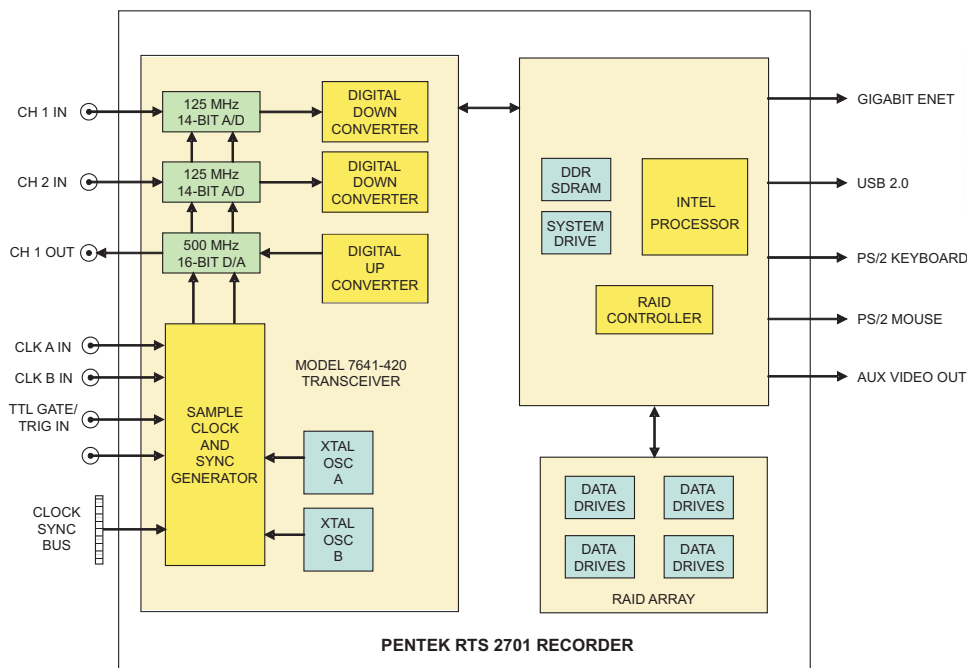


Figure 76

The Pentek RTS 2701 is a highly scalable recording and playback system in an industrial rack-mount PC server chassis. Built on the Windows XP professional workstation, it utilizes the Model 7641-420 multiband transceiver PCI module with two 14-bit 125 MHz A/Ds, ASIC DDC, and DUC with two 16-bit 500 MHz D/As.

The factory-installed IP core 420 provides a dual wideband DDC and expands the decimation range of the ASIC DDC. The core also includes an interpolation filter that expands the interpolation factor of the ASIC DUC. The Model 7641-420 combines downconverter and upconverter functions in one PCI module and offers recording and playback capabilities.

Included with this instrument is Pentek's System-Flow recording software. The RTS 2701 uses a native NTFS record/playback file format for easy access by user

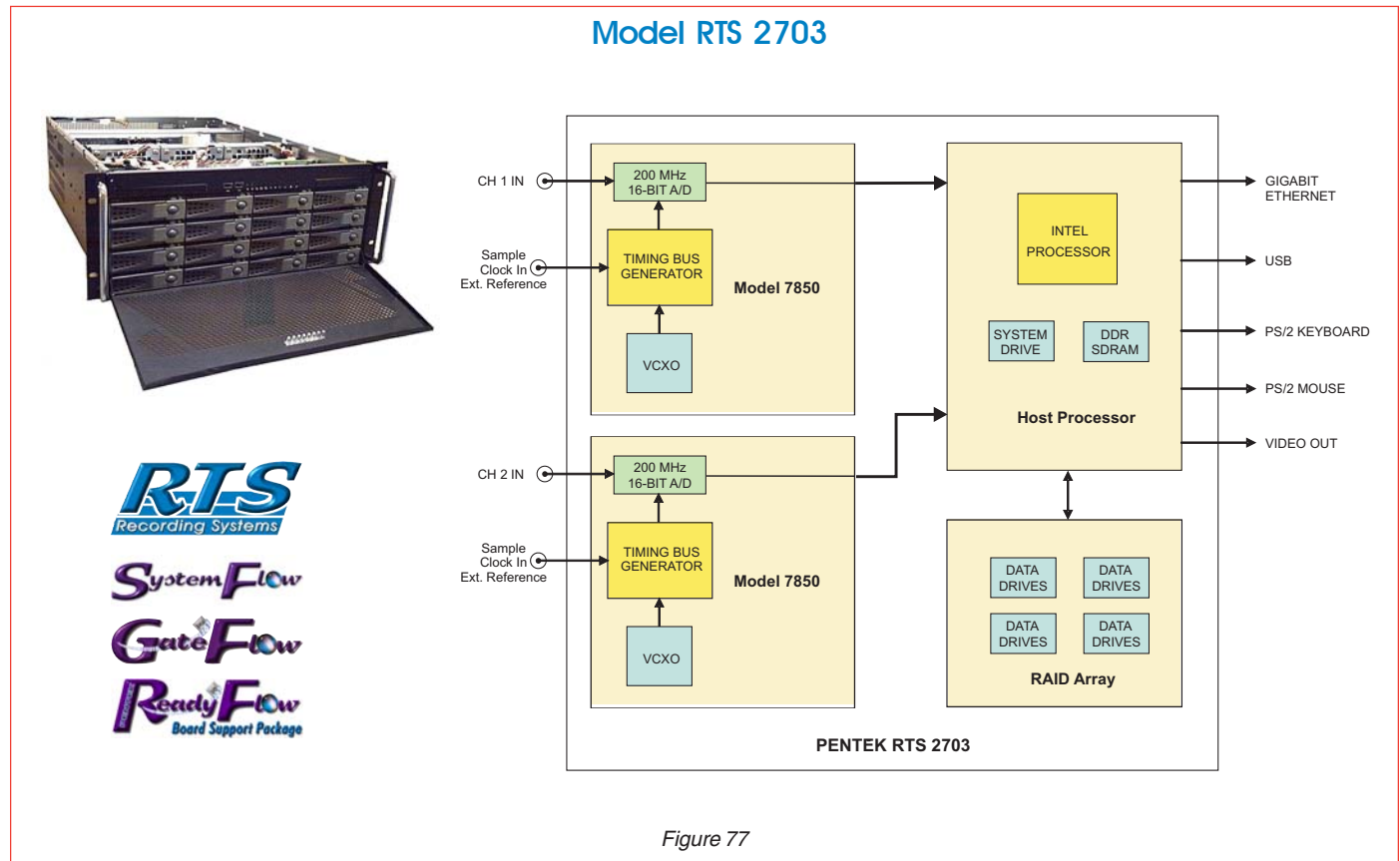
applications for analysis, signal processing, and waveform generation. File headers include recording parameter settings and time stamping so that the signal viewer correctly formats and annotates the displayed signals.

A high-performance PCI Express SATA RAID controller connects to multiple SATA hard drives to support storage to 4 terabytes and real-time sustained recording rates to 480 MB/sec.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The Pentek RTS 2701 serves equally well as a development platform for advanced research projects and proof-of-concept prototypes, or as a cost-effective strategy for deploying high-performance, multichannel embedded systems.

Products

2-Channel 200 MSample/sec Real-Time Recorder Instrument



The Pentek RTS 2703 is a turnkey recording instrument that allows the user to record and analyze two high-bandwidth signals. The RTS 2703 provides sustained, aggregate recording rates of up to 800 MB/sec, forming a powerful dual-channel 4U rack-mount recording system.

The front end of the RTS 2703 consists of two Pentek Model 7850 PCIe modules each equipped with 200 MHz 16-bit A/D converters. The RTS 2703 retains all 16 bits of each A/D sample (2 bytes), recording two signals at up to 200 MSamples/sec.

A total of 4 TB of RAID storage is provided, allowing sustained 2 TB recordings at 200 MSamples/sec simultaneously on each of two channels for over one hour.

Included with this instrument is Pentek's SystemFlow Recording Software. The RTS 2703 features a Windows-

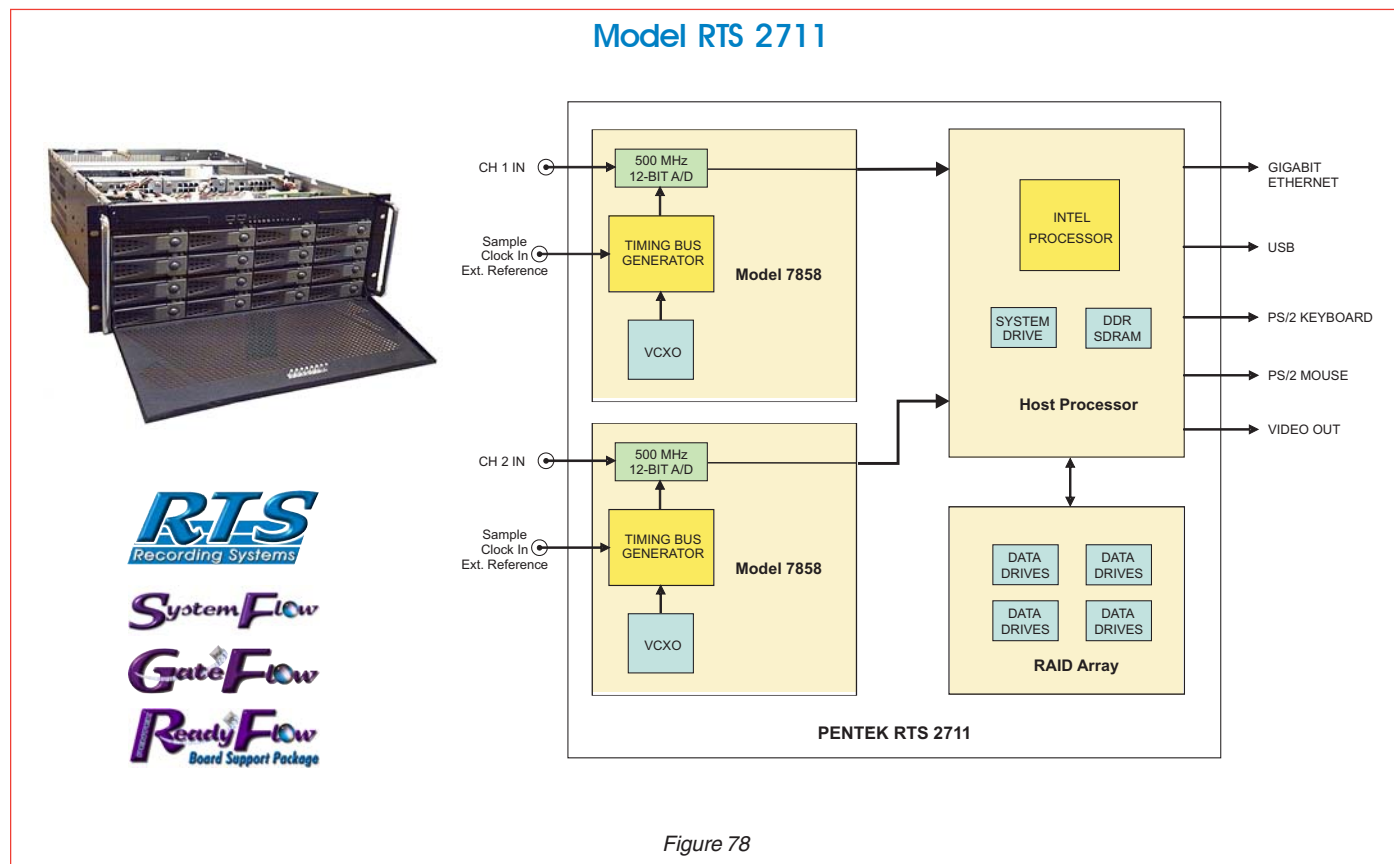
based GUI (graphical user interface) providing a simple means to configure and control the instrument. Custom configurations can be stored as profiles and later retrieved for easy selection of pre-configured settings with a single click.

Built on a Windows XP Professional workstation, users can install post processing and analysis tools to operate on the recorded data. The RTS 2703 records data to the native NTFS file system, providing immediate access to the recorded data.

Pentek's RTS 2703 provides a flexible architecture that can be easily customized to meet user needs. Multiple RAID levels, including 0, 1 and 5, provide a choice for the required level of redundancy. The total drive capacity is 4 TB using 10 drives, which are organized as two 5-drive, 2 TB arrays, one array for each A/D channel.

Products

2-Channel 500 MSample/sec Real-Time Recorder Instrument



The Pentek RTS 2711 is a turnkey recording instrument that allows the user to record and analyze two high-bandwidth signals. The RTS 2711 provides sustained, aggregate recording rates of up to 1 GB/sec forming a powerful dual-channel 4U rack-mount recording system.

The front end of the RTS 2711 consists of two Pentek Model 7858 PCIe modules equipped with 500 MHz 12-bit A/D converters. The RTS 2711 retains the eight most significant bits of each A/D sample to record two signals at 500 megasamples per second.

A total of 4 TB of RAID storage is provided, allowing sustained 2 TB recordings at 500 megasamples per second simultaneously on each of two channels for over one hour.

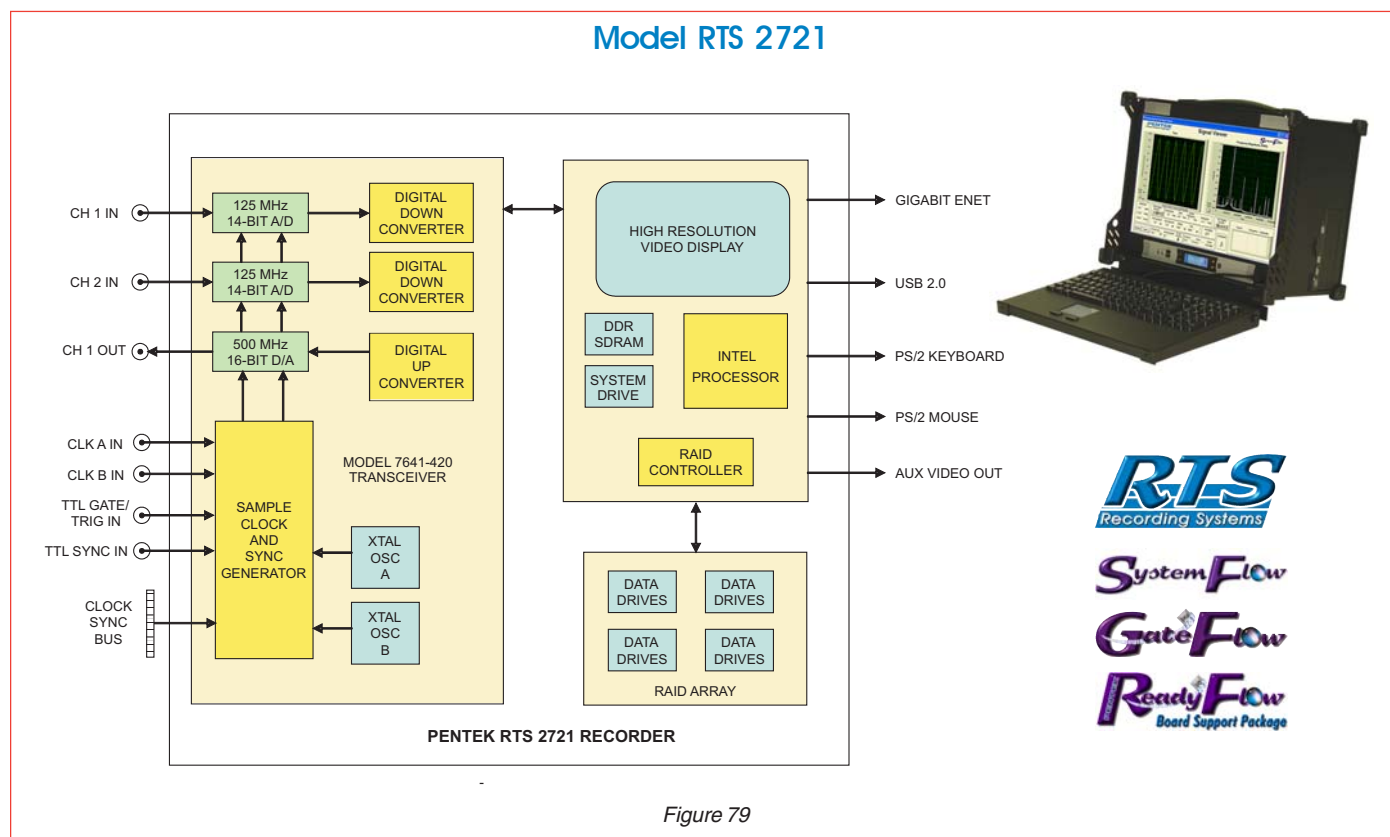
Included with this instrument is Pentek's SystemFlow Recording Software. The RTS 2711 features a Windows-

based GUI (graphical user interface) that provides a simple means to configure and control the instrument. Custom configurations can be stored as profiles and later retrieved for easy selection of preconfigured settings with a single click.

Built on a Windows XP Professional workstation, users can install post-processing and analysis tools to operate on the recorded data. The RTS 2711 records data to the native NTFS file system, providing immediate access to the recorded data.

Pentek's RTS 2711 provides a flexible architecture that can be easily customized to meet user needs. Multiple RAID levels, including 0, 1, 5, 6, 10 and 50 provide a choice for the required level of redundancy. The total drive capacity is 4 TB using 16 drives which are organized as two 8-drive, 2-TB arrays, one for each A/D channel.

Portable Real-Time Recording and Playback Transceiver Instrument



The Pentek RTS 2721 is a turnkey real-time recording and playback instrument supplied in a convenient briefcase-size package that weighs just 30 pounds. Built on the Windows XP professional workstation, it includes a dual-core Xeon processor, a high-resolution 17-inch LCD monitor and a high-performance SATA RAID controller.

The RTS 2721 utilizes the Model 7641 multiband transceiver PCI module with two 14-bit 125 MHz A/Ds, ASIC DDC, and DUC with two 16-bit 500 MHz D/As. The factory-installed IP core 420 provides a dual wideband DDC and expands the decimation range of the ASIC DDC. The core also includes an interpolation filter that expands the interpolation factor of the ASIC DUC.

The Model 7641-420 combines downconverter and upconverter functions in one PCI module and offers real-time recording capabilities.

Fully supported by Pentek's SystemFlow recording software, the RTS 2721 uses a native NTFS record/playback file format for easy access by user applications for analysis, signal processing, and waveform generation. File headers include recording parameter settings and time stamping so that the signal viewer correctly formats and annotates the displayed signals.

A high-performance PCI Express SATA RAID controller connects to multiple SATA hard drives to support storage to 3 terabytes and real-time sustained recording rates up to 480 MB/sec.

Pentek's portable recorder instrument provides a flexible architecture that is easily customized to meet special needs. Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. With its wide range of programmable decimation and interpolation, the system supports signal bandwidths from 8 kHz to 60MHz.

Products

Pentek SystemFlow® Recording Software

Model 4990

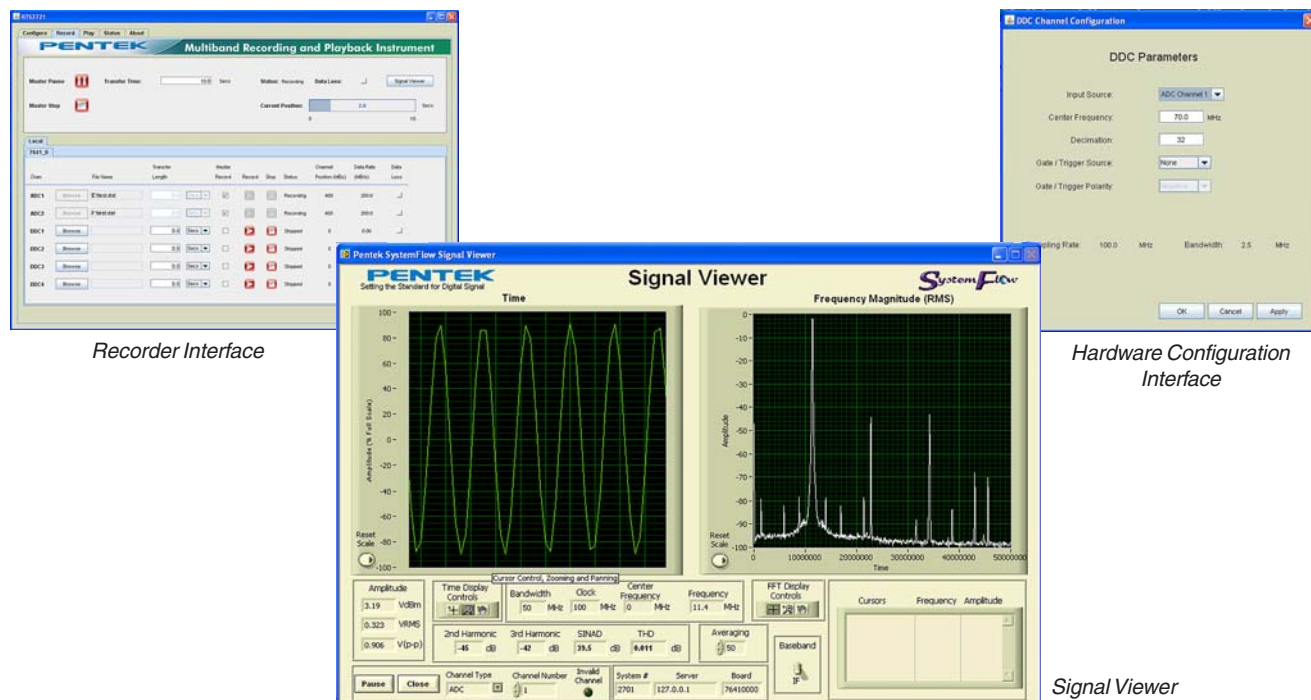


Figure 80

The Model 4990 SystemFlow Recording Software provides a rich set of function libraries and tools for controlling all Pentek RTS real-time data acquisition and recording instruments. SystemFlow software allows developers to configure and customize system interfaces and behavior.

The **Recorder Interface** includes configuration, record, playback and status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperatures and voltage levels.

The **Hardware Configuration Interface** provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The SystemFlow **Signal Viewer** includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

Products

Levels of Ruggedization for High-speed VME/VXS and PMC/XMC Pentek Products

Level	L0	L1	L2	L3	L4
Cooling	Forced Air	Forced Air	Forced Air	Conduction	Conduction
Operating Temp	0° to 50°C	0° to 50°C	-20° to 65°C	-40° to 70°C	-40° to 85°C
Storage Temp	-20° to 70°C	-40° to 100°C	-40° to 100°C	-50° to 100°C	-50° to 100°C
Sine Vibration	-	2g 20-500 Hz	2g 20-500 Hz	10g 20-2000 Hz	10g 20-2000 Hz
Random Vibration	-	0.01 g ² /Hz 20-2000 Hz	0.04 g ² /Hz 20-2000 Hz	0.1 g ² /Hz 20-2000 Hz	0.1 g ² /Hz 20-2000 Hz
Shock	-	10g, 11 ms	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity*					
No Conf Coat	0% to 95%	0% to 95%	0% to 95%	0% to 95%	0% to 95%
With Conf Coat	0% to 100%	0% to 100%	0% to 100%	0% to 100%	0% to 100%

* non-condensing

Figure 81

To make Pentek's high-speed VME/VXS and PMC/XMC products operate in harsh environments of heat, vibration, shock or altitude, five different levels of ruggedization are offered.

This chart shows the five levels and the appropriate environmental specifications for each.

Level L0 is standard commercial level for normal laboratory environments.

Levels L1 and L2 are for forced air cooling environments where temperature, shock and vibration may be a

factor. Examples of such environments are shipboard installations and military vehicles.

Levels L3 and L4 are provided for environments where air is not available to cool the boards. This could be due to very high altitudes or severe conditions of dust, moisture or sand.

Instead, the boards are put in a sealed enclosure and heat is drawn out through thermal conduction.

In the next few pages we illustrate our strategy for conduction cooling.

Products

Conduction Cooled Printed Circuit Board Design

- Thermal management must accommodate thru hole, surface mount and ball grid packaging
- Inner copper layers draw heat to the edges of the board
- Copper plated thru holes bring heat to the top and bottom surfaces

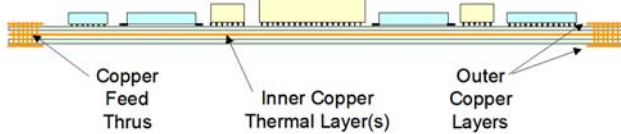


Figure 82

The printed circuit board is manufactured with layers of heavy copper planes to pull heat out to the edges of the board.

Feedthrough holes are stitched along the edges to bring the heat to the top and bottom surfaces.

Commercial L0 Model 6821 Showing Thermal Transfer Pads

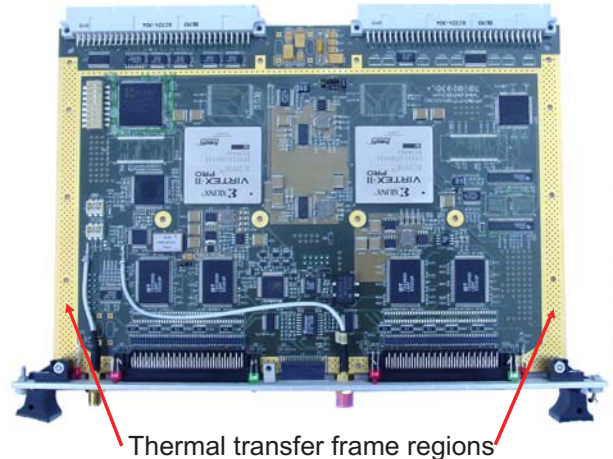


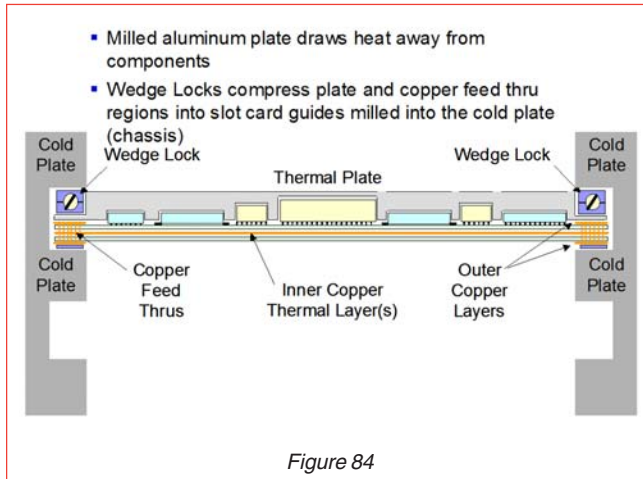
Figure 83

This shows the commercial version of the board which does not have the conduction cooling hardware installed.

Note the provisions for the thermal transfer regions along both edges that come into play for the conduction cooled version.

Products

Conduction Cooling Mechanical Hardware



For conduction cooling, an aluminum thermal plate is milled to conform to the various heights of each component.

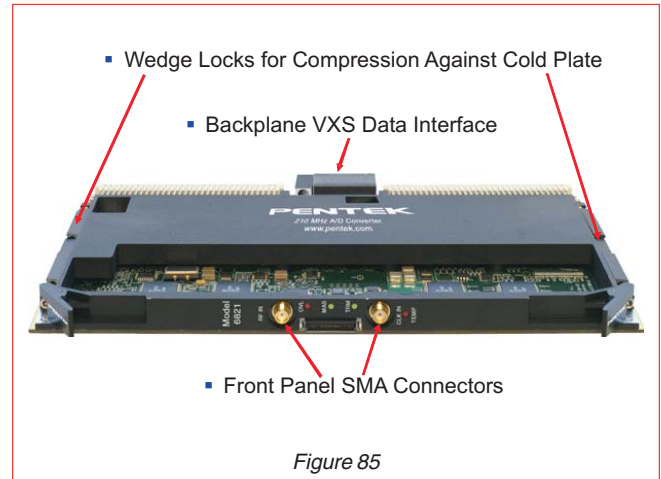
It conducts heat away from the components and towards the left and right edges of the board.

A wedge lock compresses the plate and the copper feedthrough regions into slots of the aluminum chassis cardguide to ensure good thermal contact with the slot.

Heat flows through the aluminum thermal plate and copper layers into the slots in cold plates forming the sides of the chassis.

The cold plate must be maintained below a maximum temperature by a heat exchanger or some other external cooling method.

L3 Conduction Cooled Version of Model 6821



Here's a photo of the L3 conduction cooled version of the Model 6821 A/D Converter.

Also, notice the VXS P0 connector in the middle of the back edge of the board.

Applications

8-Channel 125 MHz Data Acquisition System

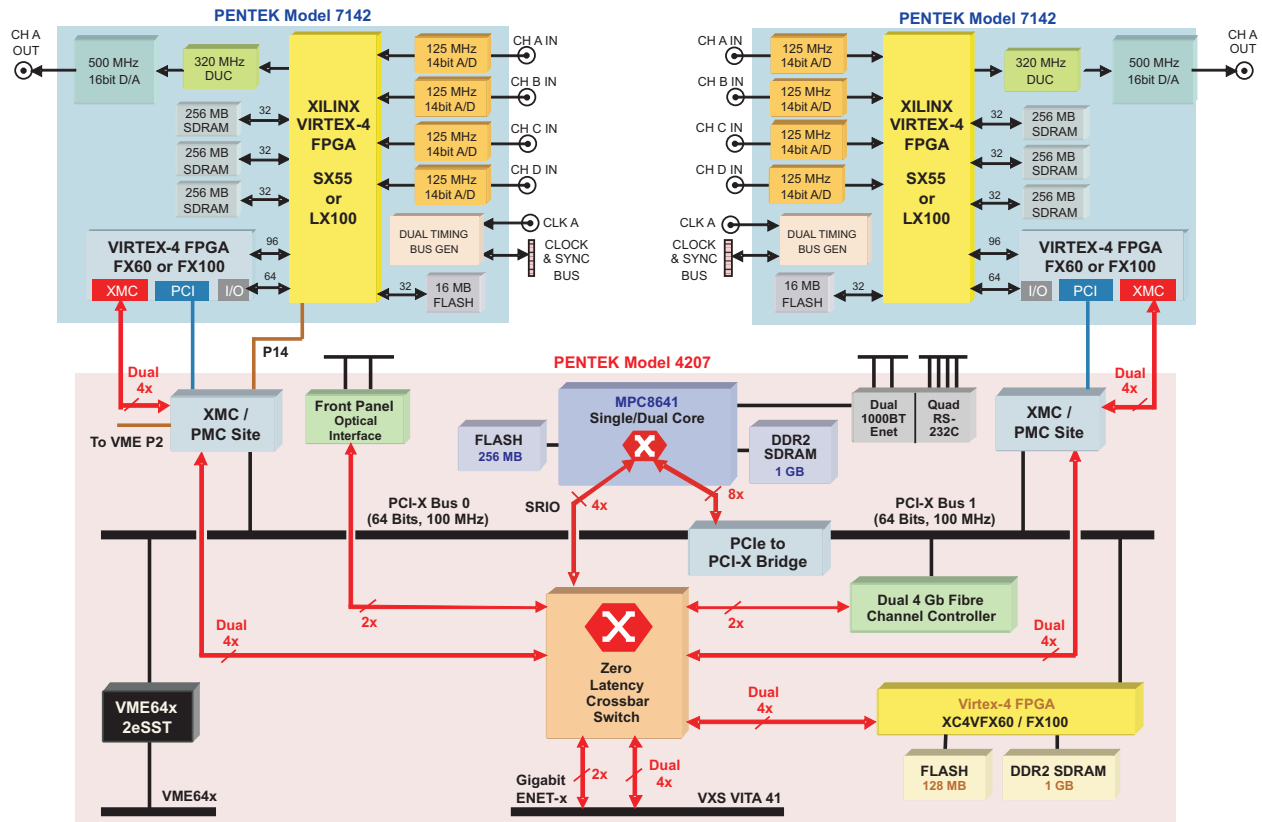


Figure 86

This system digitizes eight analog input signals with bandwidths up to about 60 MHz using the four LTC2255 125 MHz 14-bit A/D converters on each PMC/XMC module. These transformer-coupled inputs accommodate both baseband and IF signals at frequencies up to 140 MHz.

Two wideband analog outputs are generated by the one DAC5686 DUC (digital upconverter) on each PMC module. Each DUC contains a mixer and local oscillator for frequency translation of baseband signals to IF frequencies up to 140 MHz and higher. Each DUC also contains a 16-bit 500 MHz D/A converter

that delivers the analog output to a front panel coaxial connector.

Signal processing resources on each PMC/XMC module include either the SX55 for high-performance DSP algorithms or the LX100 for logic intensive algorithms, depending on the option ordered.

For large multichannel systems, the 7142 modules can be synchronized using the front panel sync/gate LVDS bus. In this way, up to 320 A/D channels can be clocked, triggered and gated synchronously using the Pentek Model 9190 Clock and Sync Generator.

Applications

Dual-Channel 215 MHz VXS Recording System

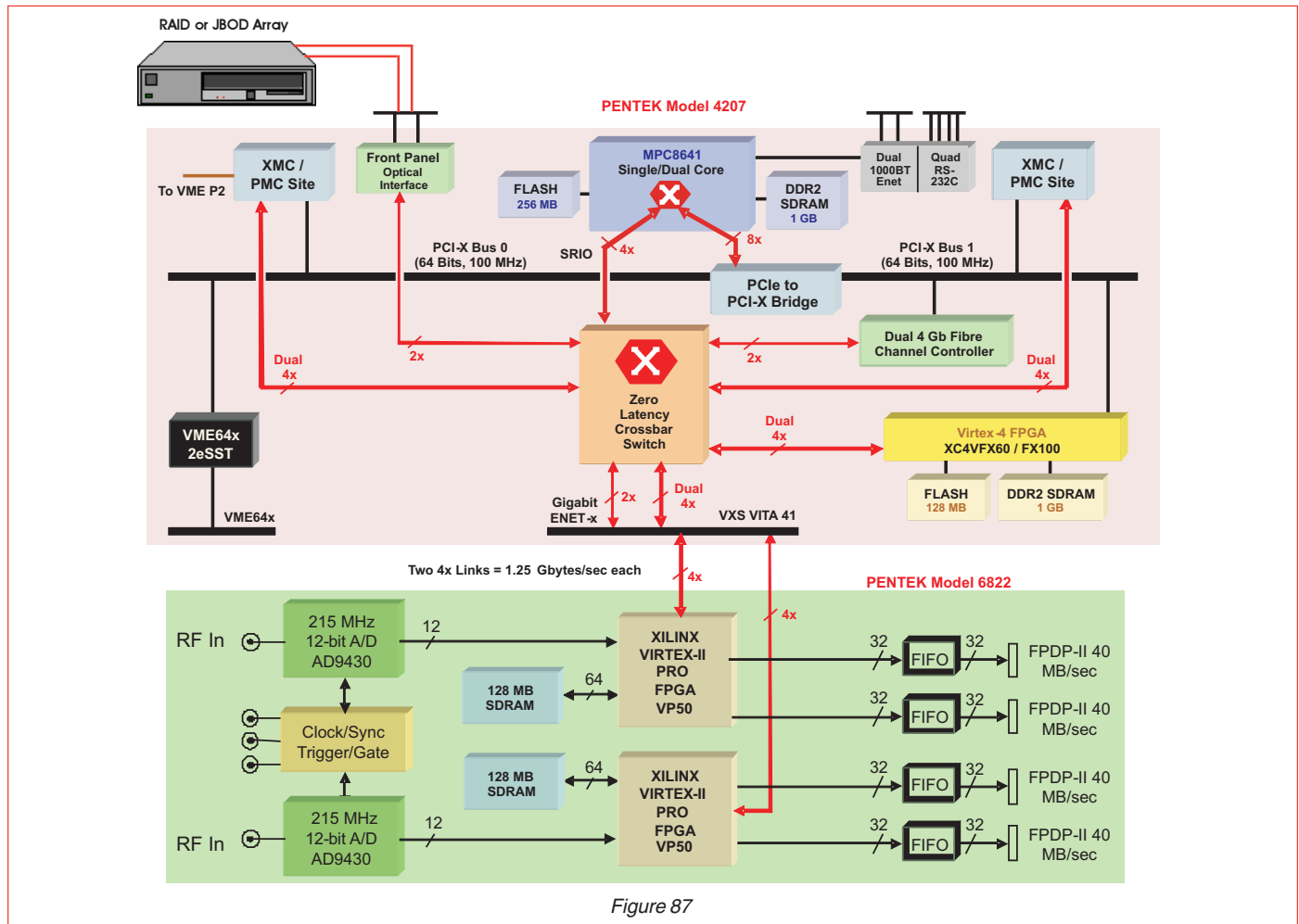


Figure 87

The Model 6822 provides two 215 MHz 12-bit A/D converters capable of digitizing two analog inputs with bandwidths to 100 MHz with a 215 MHz sampling rate. Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking filters.

Complete gating and triggering functions support pulsed signal acquisition for radar applications.

After data is buffered in SDRAM, it can be transferred across two 4X VXS links, each operating at up to 1.25 GB/sec.

The Model 4207 VXS ports accept data into SDRAM buffers for recording onto the RAID or JBOD disk array at rates up to 640 MB/sec.

The duty cycle characteristic of pulsed radar signals allows elastic memory buffering to average the peak rates to accommodate continuous real-time recording of the pulses.

This platform offers a wideband acquisition and recording system ideal for radar and advanced communication projects.

Applications

4-Channel Software Radio Transceiver System

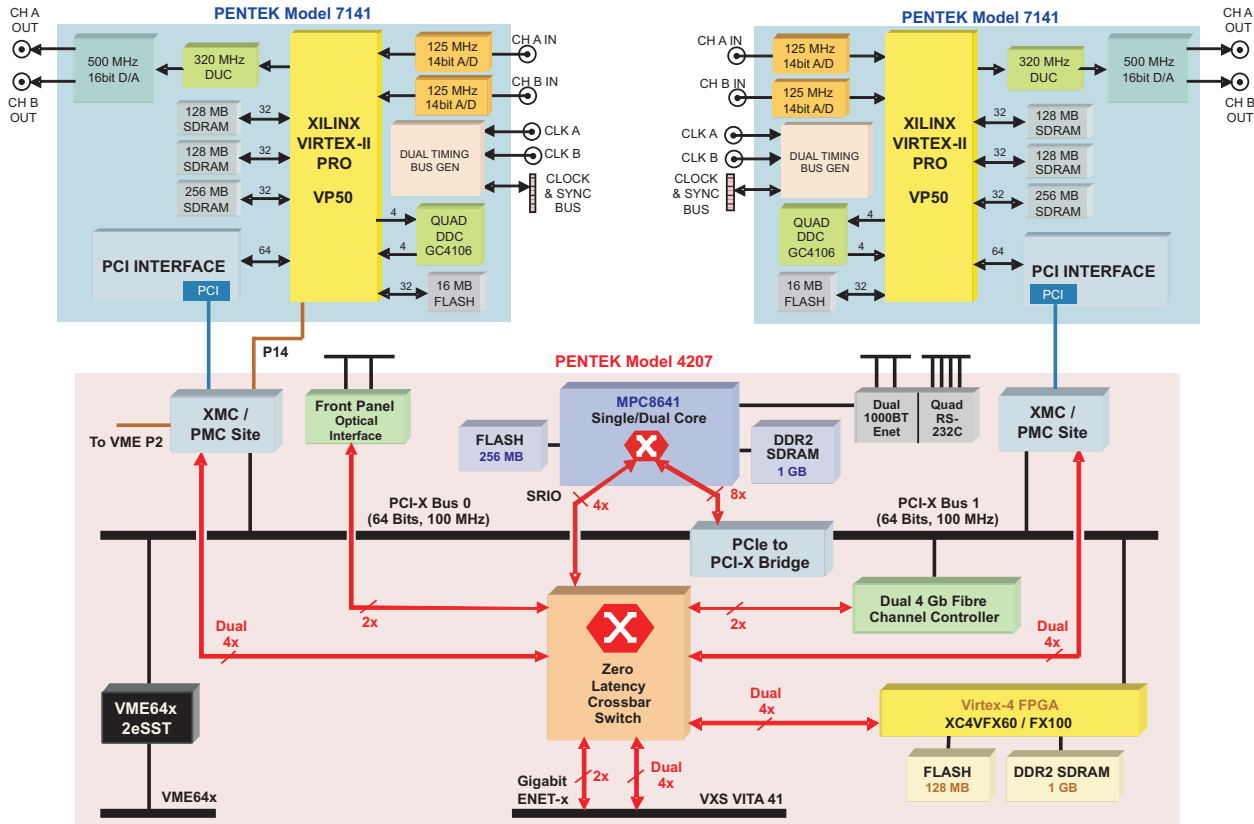


Figure 88

This system accepts four analog inputs from baseband or IF signals with bandwidths up to 50 MHz and IF center frequencies up to 150 MHz. A total of eight DDC channels are independently tunable across the input band and can deliver downconverted output signal bandwidths from audio up to 2.5 MHz.

Four analog outputs can deliver baseband or IF signals with bandwidths up to about 50 MHz and IF center frequencies up to 100 MHz. The system supports four independent D/A channels or two upconverted channels with real or quadrature outputs.

Signal processing resources include the Freescale MPC8641 Altivec processor and an FX60 or FX100 on the 4207 plus a VP-50 FPGA on each PMC module.

Using these on-board processing resources this powerful system can process analog input data locally and deliver it to the analog outputs. It can also be used as a pre- and post-processing I/O front end for sending and receiving data to other system boards connected over the VMEbus or through switched fabric links using the VXS interface.

Ruggedized and conduction-cooled versions of the boards used in this system are available.

Applications

512-Channel Software Radio Recording System in a Single VMEbus Slot

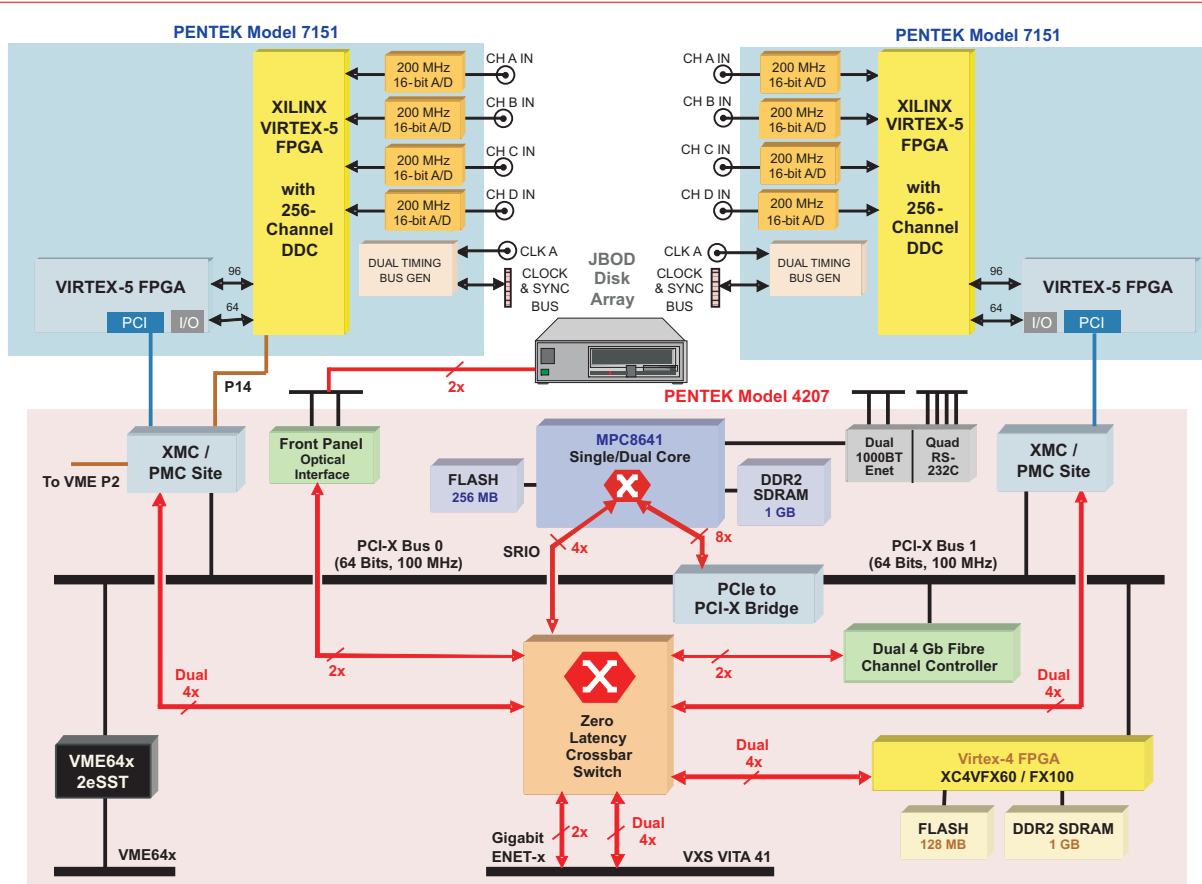


Figure 89

The Model 7151 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 256 DDCs has an independent 32-bit tuning frequency setting.

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

A dual 4-Gbit Fibre Channel copper interface allows wideband A/D data or DDC outputs from all

512 channels to be recorded in real time to a RAID or JBOD disk array at aggregate rates up to 640 MB/sec.

Pentek's SystemFlow® software presents an intuitive graphical user interface (GUI) to set up the DDC channels and recording mode. The GUI executes on a Windows host PC connected to the 4207 via Ethernet.

A SystemFlow signal viewer on the PC allows previewing of data prior to recording and viewing of recorded data files in both time and frequency domains. Files can be moved between the Fibre Channel disk and the PC over Ethernet.

This system is ideal for downconverting and capturing real time signal data from a very large number of channels in an extremely compact, low cost system.

Applications

8-Channel Beamforming System

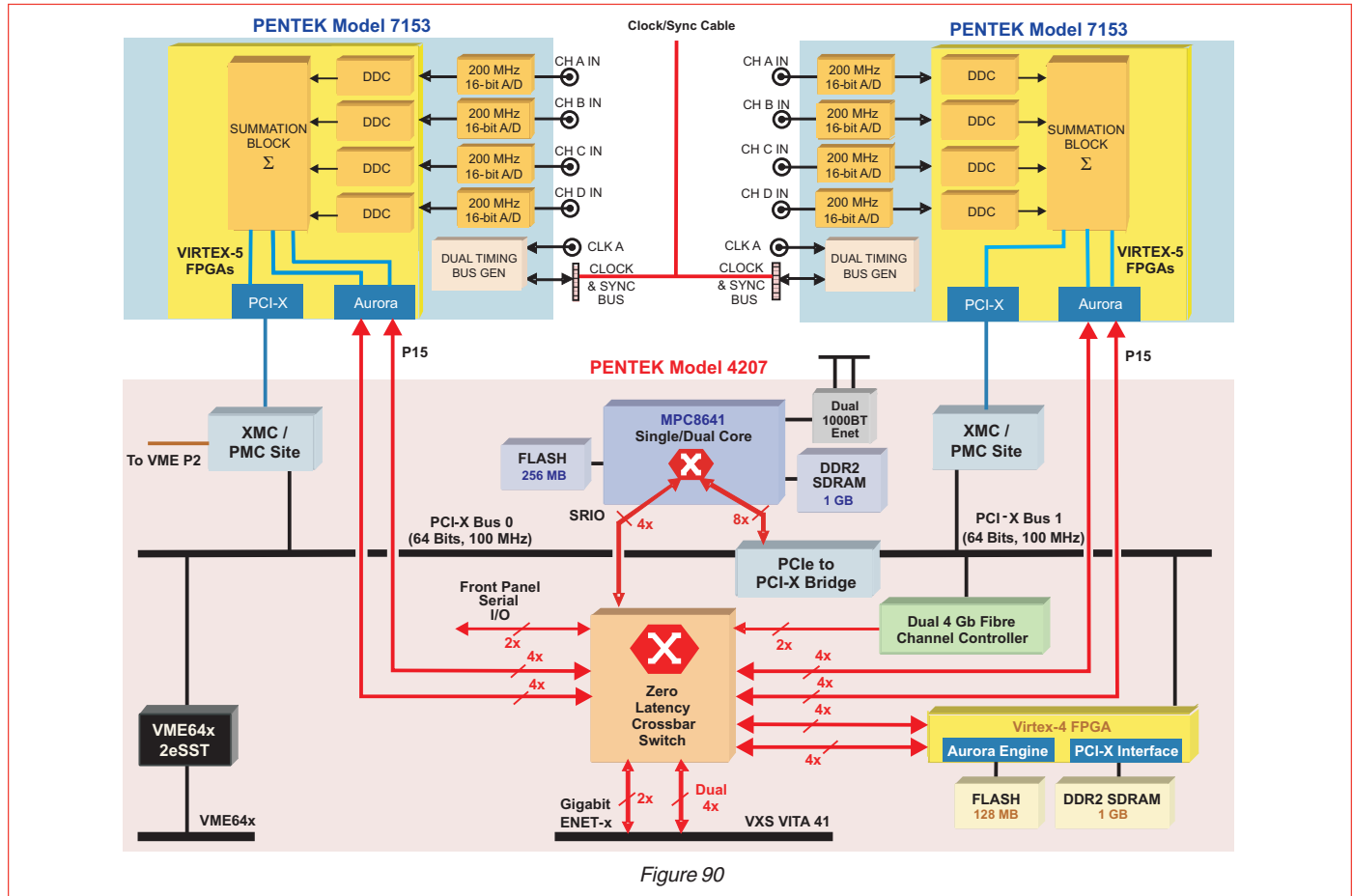


Figure 90

Two Model 7153 Beamformer PMC/XMC modules are installed on the Model 4207 I/O Processor board. The eight signals to be beamformed are connected to the eight analog inputs of these modules. Joining the two 7153 modules is a clock/sync cable that synchronizes the DDCs and guarantees synchronous sampling across all eight channels.

Signals from the first four channels of the left 7153 module are summed in the left summation block; signals from the second four channels of the right 7153 are summed in the right summation block. The summation output from the left XMC module is delivered using the Aurora 4x link into one port of the crossbar switch. Each red 4x link is capable of data rates up to 1.25 GBytes/sec. The left 4-channel sum is connected through the crossbar switch and delivered into the summation input port of the right XMC module.

The Aurora summation from the left four channels is combined with the right four channels and then delivered to the crossbar switch from the right summation output port. The eight-channel combined sum is delivered through the crossbar switch into the Aurora engine implemented in the Virtex-4 FPGA of the 4207 processor board.

This Aurora engine decodes the stream and delivers it to a designated block in the DDR2 memory attached to the FPGA. The PCI-X interface in this FPGA presents the SDRAM memory as a mapped resource appearing on the processor PCI-X bus 1. The Power PC reads the data from the FPGA DDR2 memory across the PCI-X bus, creates the beamformed pattern display and presents it via its front panel gigabit Ethernet port to an attached PC for display.

Summary

Summary

- A/D Technology and Markets
- Sampling and Filtering Techniques
- New FPGA Technology for A/Ds
- Serial Switched Fabrics for A/Ds
- High Speed A/D Products
- Applications
- Summary

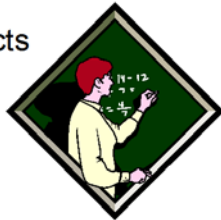


Figure 91

As we have seen, quite a bit of technology needs to surround and support these new high-speed A/D converters in order to deploy them successfully in real-time systems.

A complete signal acquisition plan must be developed. It should include frequency content of the signal, voltage levels, accuracy, and bandwidth.

Processing these extremely high-speed sample streams is often possible only with FPGA technology.

FPGAs can also help implement interfaces to switched serial fabrics so that data can be successfully delivered to other parts of the system.

We looked at several product examples and then at several applications that illustrate the impressive variety of tasks and systems made possible by this technology. For more information on the Pentek products described in this handbook, use the links provided in the next page.

For More Information....

- Vendors
 - Pentek (DSP, Software Radio): www.pentek.com
 - Pentek (FPGA Resources): www.pentek.com/gateflow
 - Xilinx (Fabric IP Cores, Gigabit I/O): www.xilinx.com
 - Altera (Fabric IP Cores, Gigabit I/O): www.altera.com
 - Bustronic (VXS Backplane): www.bustronic.com
 - Analog Devices (A/D Converters): www.analog.com
 - Atmel (A/D Converters): www.atmel.com
- Trade and Standards Organizations
 - VXS and XMC: www.vita.com
 - RapidIO: www.rapidio.org
 - Infiniband: www.infinibandta.org
 - HyperTransport: www.hypertransport.org
 - Star Fabric: www.starfabric.org
 - PCI Express: www.intel.com/technology/pciexpress/devnet/

Figure 92

Here's a list of useful links you can use to check out more details about the manufacturers' devices used in the products we have discussed.

For specifications for VXS and XMC, the switched fabric for PMC, visit the VITA (VMEbus International Trade Organization) website.

You can also learn more about the switched serial fabric standards and protocols from the respective trade and technical organizations for each of them.

Links



The following links provide you with additional information about the Pentek products presented in this handbook: just click on the Model number. Links are also provided to other handbooks or brochures that may be of interest to you in your development projects.

Model	Description	Page
4207	MPC8641 PowerPC Processor with Virtex-4 FPGA - VME/VXS	35
6821	215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS	36
6822	Dual 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS	37
6826	Dual 2 GHz, 10-bit A/D with Virtex-II Pro FPGAs - VME/VXS	38
7141	Multiband Digital Transceiver with Virtex-II Pro FPGAs - PMC/XMC	39
7241	Multiband Digital Transceiver with Virtex-II Pro FPGAs - 6U cPCI	39
7341	Multiband Digital Transceiver with Virtex-II Pro FPGAs - 3U cPCI	39
7641	Multiband Digital Transceiver with Virtex-II Pro FPGAs - PCI	39
7741	Multiband Digital Transceiver with Virtex-II Pro FPGAs - Full-length PCIe	39
7841	Multiband Digital Transceiver with Virtex-II Pro FPGAs - Half-length PCIe	39
5341	Multiband Transceiver with Virtex-II Pro FPGA - 3U VPX	39
7142	Multichannel Transceiver with Virtex-4 FPGAs - PMC/XMC	40
7242	Multichannel Transceiver with Virtex-4 FPGAs - 6U cPCI	40
7342	Multichannel Transceiver with Virtex-4 FPGAs - 3U cPCI	40
7642	Multichannel Transceiver with Virtex-4 FPGAs - PCI	40
7742	Multichannel Transceiver with Virtex-4 FPGAs - Full-length PCIe	40
7842	Multichannel Transceiver with Virtex-4 FPGAs - Half-length PCIe	40
5342	Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX	40
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC	41
7250	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 6U cPCI	41
7350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U cPCI	41
7650	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCI	41
7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length PCIe	41
7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Half-length PCIe	41
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX	41
7151	Quad 200 MHz, 16-bit A/D with 256-Channel DDC Core - PMC	42
7251	Quad 200 MHz, 16-bit A/D with 256-Channel DDC Core - 6U cPCI	42
7351	Quad 200 MHz, 16-bit A/D with 256-Channel DDC Core - 3U cPCI	42
7651	Quad 200 MHz, 16-bit A/D with 256-Channel DDC Core - PCI	42
7751	Quad 200 MHz, 16-bit A/D with 256-Channel DDC Core - Full-length PCIe	42
7851	Quad 200 MHz, 16-bit A/D with 256-Channel DDC Core - Half-length PCIe	42
5351	Quad 200 MHz, 16-bit A/D with 256-Channel DDC Core - 3U VPX	42
7153	Quad 200 MHz, 16-bit A/D with 4-Channel DDC Core - PMC/XMC	43
7253	Quad 200 MHz, 16-bit A/D with 4-Channel DDC Core - 6U cPCI	43
7353	Quad 200 MHz, 16-bit A/D with 4-Channel DDC Core - 3U cPCI	43
7653	Quad 200 MHz, 16-bit A/D with 4-Channel DDC Core - PCI	43
7753	Quad 200 MHz, 16-bit A/D with 4-Channel DDC Core - Full-length PCIe	43
7853	Quad 200 MHz, 16-bit A/D with 4-Channel DDC Core - Half-length PCIe	43
5353	Quad 200 MHz, 16-bit A/D with 4-Channel DDC Core - 3U VPX	43

More links on the next page ➤

Links



Model	Description	Page
7156	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC	44
7256	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI	44
7356	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI	44
7656	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI	44
7756	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length PCIe	44
7856	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length PCIe	44
5356	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX	44
7158	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC	45
7258	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI	45
7358	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI	45
7658	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI	45
7758	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length PCIe	45
7858	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length PCIe	45
5358	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX	45
71620	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA	46
71660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - XMC	47
6890	2.2 GHz Clock, Sync and Gate Distribution Board - VME	48
6891	System Synchronizer and Distribution Board - VME	49
7190	Multifrequency Clock Synthesizer - PMC	50
7290	Multifrequency Clock Synthesizer - 6U cPCI	50
7390	Multifrequency Clock Synthesizer - 3U cPCI	50
7690	Multifrequency Clock Synthesizer - PCI	50
7790	Multifrequency Clock Synthesizer - Full-length PCIe	50
7890	Multifrequency Clock Synthesizer - Half-length PCIe	50
5390	Multifrequency Clock Synthesizer - 3U VPX	50
9190	Clock and Sync Generator for I/O Modules	51
RTS 2701	Rack-mount Real-Time Recording and Playback Transceiver Instrument	52
RTS 2703	2-Channel 200 MSample/sec Real-Time Recorder Instrument	53
RTS 2711	2-Channel 500 MSample/sec Real-Time Recorder Instrument	54
RTS 2721	Portable Real-Time Recording and Playback Transceiver Instrument	55
4990	Pentek SystemFlow Recording Software	56
Handbooks and Brochures		
Click here	Software Defined Radio Handbook	
Click here	Putting FPGAs to Work in Software Radio Systems Handbook	
Click here	High-Speed Switched Serial Fabrics Improve System Design Handbook	
Click here	Model 4207 MPC8641 PowerPC Processor Board Brochure	